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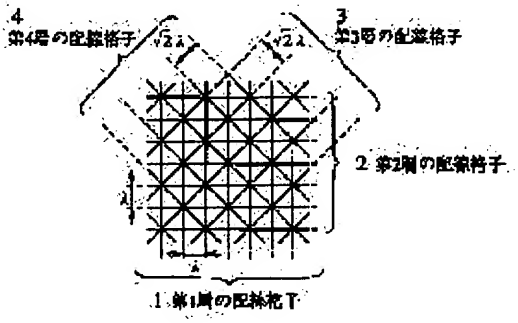
(54) SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE, WIRING METHOD THEREOF AND CELL ARRANGEMENT METHOD

(57)Abstract:

PROBLEM TO BE SOLVED: To reduce delay in a circuit and realize improvement of noise resis tance in a semiconductor integrated circuit of a multilayer wiring structure with a wiring layer of an oblique wiring lattice.

SOLUTION: An n-th (n≥2) layer wiring is provided with reference wiring layers 1, 2 forming an X-Y direction reference wiring lattice by a wiring of an m-th (m≥2) layer at right angles to an (n-1)-th layer wiring and oblique wiring layers 3, 4 which intersect at 45° or 135° to a reference wiring lattice by an (m+1)-th layer wiring and an (m+2)-th layer wiring which intersect at right angles mutually and whose wiring pitch between the (m+1)-th



layer wiring and the (m+2)-th layer wiring is set √2 times to a wiring pitch between wiring of each reference wiring layer and whose wiring width is set to √2 times the wiring width of each reference wiring layer.

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* NOTICES *

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CLAIMS

[Claim(s)]
[Claim 1] With wiring of m (m>=2) layer with which it is formed in the upper layer of the semiconductor region in which two or more unit element children were formed, and said semiconductor region, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually With the m+1st-layer wiring and the m+2nd-layer wiring which are located in the criteria wiring layer which forms the criteria wiring grid of the direction of X-Y, and the upper layer of said criteria wiring layer, and intersect perpendicularly mutually The slanting wiring layer which forms the slanting wiring grid which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring grid is provided. Said slanting wiring layer While being set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring Semiconductor integrated circuit equipment with which wiring width of face of the m+1st-layer wiring and said m+2nd-layer wiring is characterized by being set up root2 twice to the wiring width of face of each layer of said criteria wiring layer.
[Claim 2] Said slanting wiring layer is semiconductor integrated circuit equipment according to claim 1 with which the wiring thickness is characterized by being set up root2 twice of the wiring thickness of said criteria wiring grid.
[Claim 3] It is semiconductor integrated circuit equipment according to claim 1 or 2 which said criteria wiring layer and said slanting wiring layer constitute a wiring channel field, and is characterized by preparing said wiring channel field in the direction parallel to the cel low which has arranged to seriate the logic cell which consists of said unit element child.
[Claim 4] For said beer hall, 3 is [claim 1 to which it is characterized by for wiring of said criteria wiring layer and wiring of said slanting wiring layer establishing the beer hall for wiring connection in these crossover parts, and the cross section being the configuration of either a hexagon, an octagon and a parallelogram thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 5] 4 is [claim 1 which said two or more unit element children constitute a cel, and is characterized by said cel having the obstruction field which is defined by the configuration where it met in the wiring direction of said slanting wiring grid, and where wiring is not performed thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 6] For wiring of said slanting wiring layer, 5 is [claim 1 characterized by constituting the part as power-source wiring for current supply thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 7] Said two or more unit element children constitute the cel which consists of said two or more unit element children. Said cel A clock signal is supplied by the wiring path of a tree mold. Said tree type of wiring path The 1st connection by the path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 1st and 2nd points, The 2nd connection by the path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 3rd and 4th points 6 is [claim 1 characterized by being constituted combining the unit wiring configuration constituted by connecting with wiring of said criteria wiring layer thru/or] semiconductor integrated

circuit equipment of a publication either.
[Claim 8] the [which the above-mentioned semiconductor integrated circuit equipment is further located in the upper layer of said slanting wiring layer, and intersects perpendicularly mutually] -- with p-1 (p>=2) layer wiring and the p-th-layer wiring The up wiring layer which forms the up wiring grid which crosses at the include angle of 45 degrees or 135 degrees to said slanting wiring grid or the p-th-2nd-layer wiring is provided. Said up wiring layer While being set up root2 twice to the wiring pitch of said the p-th-2nd-layer wiring between wiring of each layer of said slanting wiring layer, the wiring pitch during wiring of each class 7 is [claim 1 to which wiring width of face of wiring of each class is characterized by being set up root2 twice to the wiring width of face of wiring of each layer of said slanting wiring layer, or said the p-th-2nd-layer wiring thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 9] For said slanting wiring layer, 8 is [claim 1 characterized by wiring global wiring covering the whole chip in general thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 10] Said criteria wiring layer is semiconductor integrated circuit equipment according to claim 9 characterized by wiring local wiring other than said global wiring.
[Claim 11] It is semiconductor integrated circuit equipment according to claim 9 or 10 characterized by having the output terminal configuration in which wiring and direct continuation of said slanting wiring layer are possible when said two or more unit element children should constitute a cel and direct continuation of said cel should be carried out to said global wiring.
[Claim 12] The above-mentioned semiconductor integrated circuit equipment possesses further a flip-flop circuit and PLL (Phase Locked Loop) arranged at the corner of a chip. A clock signal is supplied to said flip-flop circuit by the wiring path of a tree mold. Said tree type of wiring path Near the chip center, connection is carried out using wiring of said slanting wiring layer from said PLL. 11 is [claim 1 characterized by carrying out connection hierarchical so that RC product may be made to balance through a buffer cel to said flip-flop circuit near / said / the chip center thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 13] 12 is [claim 1 which the above-mentioned semiconductor integrated circuit equipment possesses further the SRAM circuit which uses wiring of said criteria wiring layer for wiring of the interior, and is characterized by wiring wiring with which said slanting wiring layer passes through said SRAM circuit top thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 14] 13 is [claim 1 which said criteria wiring layer is constituted by three layers, and is characterized by wiring the 1st-layer wiring and the 3rd-layer wiring of said criteria wiring layer in the direction parallel to the cel low which has arranged to seriate the logic cell which consists of said unit element child thru/or] semiconductor integrated circuit equipment of a publication either.
[Claim 15] For said criteria wiring layer, 13 is [claim 1 characterized by being constituted by two-layer thru/or] the semiconductor integrated circuit of a publication either.
[Claim 16] The component of a semiconductor integrated circuit with wiring of m (m>=2) layer with which it is the semiconductor integrated circuit wiring approach of wiring, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer While being set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring The semiconductor integrated circuit wiring approach characterized by including the step which the wiring width of face of the m+1st-layer wiring and said m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring width of face of each layer of said criteria wiring layer.
[Claim 17] The above-mentioned semiconductor integrated circuit wiring approach is the semiconductor integrated circuit wiring approach according to claim 16 which carries out [containing the step which inserts the buffer cel for signal magnification in the step which extracts the wiring network which produces the delay which exceeds a predetermined time delay further out of the wiring network which

said criteria wiring layer constitutes, and a location connectable with wiring of said slanting wiring grid on said extracted wiring network, and] as the description.
[Claim 18] The above-mentioned semiconductor integrated circuit wiring approach is the semiconductor integrated circuit wiring approach according to claim 16 or 17 characterized by including the step which defines further the cel which consists of said two or more unit element children, and the step which defines the obstruction field where wiring is not performed in said cel by the configuration where it met in the wiring direction of said slanting wiring layer.
[Claim 19] Said obstruction domain-defined step is the semiconductor integrated circuit wiring approach according to claim 18 characterized by arranging said m+1st-layer wiring or said m+2nd-layer wiring near [the] the corner.
[Claim 20] For the above-mentioned semiconductor integrated circuit wiring approach, 19 is [claim 16 which is wiring of said either of m layers of said criteria wiring layer, and is further characterized by to include the step which replaces the predetermined part in the middle of one wiring of said wiring of two with wiring of said slanting wiring layer when one wiring exerts a noise on wiring of another side among parallel wiring of two belonging to the same layer thru/or] the semiconductor integrated circuit wiring approach of a publication either.
[Claim 21] The above-mentioned semiconductor integrated circuit wiring approach is the semiconductor integrated circuit wiring approach according to claim 20 characterized by including the step which inserts a buffer cel further into the path of wiring of said slanting wiring layer used for said replacement.

[Claim 22] With wiring of m (m>=2) layer with which it is the cel configuration method which arranges a cel, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually on a semiconductor integrated circuit With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The cel configuration method characterized by including the step which arranges the cel which consists of two or more unit element children based on the predetermined cutting method using the cutline of the direction of X-Y corresponding to the wiring direction of said criteria wiring layer, and the cutline of the direction of slant corresponding to the wiring direction of said slanting wiring layer.
[Claim 23] The step which sets up the 1st path formed so that the above-mentioned semiconductor integrated circuit wiring approach might approach each other in the wiring top of said slanting wiring layer from the 1st and 2nd points further, The step which sets up the 2nd path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 3rd and 4th points, The step which forms the unit wiring configuration constituted by connecting said the 1st path and said 2nd path with wiring of said criteria wiring layer, 22 is [claim 16 characterized by including the step which forms the wiring path of the tree mold which supplies a clock signal in the cel which consists of said two or more unit element children combining said unit wiring configuration thru/or] the semiconductor integrated circuit wiring approach of a publication either.
[Claim 24] The component of a semiconductor integrated circuit with wiring of m (m>=2) layer with which it is the semiconductor integrated circuit wiring approach of wiring, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The step connected near the chip center using wiring of said slanting wiring layer from PLL (Phase Locked Loop) arranged at the corner of a chip, The semiconductor integrated circuit wiring approach characterized by including the step

connected hierarchical so that RC product may be made to balance through a buffer cel to said flip-flop circuit in said chip near [said] the chip center.
[Claim 25] The component of a semiconductor integrated circuit with wiring of m (m>=2) layer with which it is the semiconductor integrated circuit wiring approach of wiring, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The semiconductor integrated circuit wiring approach characterized by including the step which forms the SRAM circuit which uses wiring of said criteria wiring layer for wiring of the interior, and the step which forms wiring which passes through said SRAM circuit on said slanting wiring layer.

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] This invention relates to the semiconductor integrated circuit equipment, the semiconductor integrated circuit wiring approach, and cel configuration method which have multilayer-interconnection structure. In the semiconductor integrated circuit with which the wiring layer of the wiring grid of the direction of slant was especially formed in the upper layer of the wiring layer of the wiring grid of the direction of X-Y, it is related with the semiconductor integrated circuit and the semiconductor integrated circuit wiring technique of realizing reduction of delay of a circuit, and improvement in noise resistance.
[0002]
[Description of the Prior Art] The method which accumulates the wiring layer which intersects perpendicularly on the upper layer has been taken by the multilayer-interconnection structure of LSI by a conventional standard cell or a conventional gate array method. That is, as it says that the 1st layer and the 2nd layer intersect perpendicularly and the 2nd layer and the 3rd layer intersect perpendicularly, it is the configuration that the n-1st layer and the n-th layer intersect perpendicularly. In the multilayer-interconnection structure where such each class intersects perpendicularly, when connecting two points of the direction of a vertical angle, the point which separated by Euclidean distance will be connected. For this reason, wiring of the die length more than one twice [root2] the distance of a slant range is needed. Therefore, the multilayer-interconnection structure of a rectangular mold had produced the overhead also in delay characteristics also in degree of integration.
[0003] However, in case an LSI wiring design is carried out on a computer, the technique of wiring by the rectangular coordinate system is simple in algorithm. For this reason, on the computer, the above-mentioned overhead was disregarded and the wiring design was performed.
[0004] However, the delay component resulting from wiring structure has come to influence the performance of the whole circuit as detailed-ization of circuit structure progresses. It is impossible for this reason, to disregard the overhead by the above-mentioned wire length becoming long.
[0005] Specifically, the delay component which originates in wiring resistance the 1st occupies the great portion of critical path delay. Thus, the effect which a wire length has on circuit performance is increasing.
[0006] Moreover, the coupling capacity during wiring which adjoins rather than the capacity of an opposite substrate of the items of the load-carrying capacity which originates [2nd] in wiring is more dominant. For this reason, it is an important element for raising circuit performance how the capacity during adjoining wiring is mitigated.
[0007] Furthermore, coupling noise **** malfunction which originates in the coupling capacity during this wiring the 3rd is also aggravated. In the wiring structure where all conventional wiring intersects perpendicularly especially, it is between wiring which adjoins within the same layer and runs in parallel, and when doing effect mutually, even if it replaces wiring with other wiring layers, it will run in parallel by the upper and lower sides too. For this reason, it is difficult to mitigate the coupling capacity during

wiring which runs in parallel within this layer.
[0008] In addition to the wiring structure which intersects perpendicularly, in relation to rectangular mold multilayer-interconnection structure, the wiring technique which shortens a wire length using wiring of the direction of slant (45 degrees or 135 degrees) is proposed. For example, the wiring technique of this direction of slant is indicated by automatic-layout approach" of a JP,5-102305,A" semiconductor integrated circuit. This conventional technique is explained.
[0009] Drawing 28 is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit equipment of the conventional technique using wiring of this direction of slant.
[0010] This wiring structure forms the wiring grid of the direction of slant as another layer on the layer which constitutes rectangular coordinates. 401 in drawing 28 is the wiring grid (grid) of the 1st layer, it intersects perpendicularly with the upper layer, and the wiring grid 402 of the 2nd layer is formed. Furthermore, the 1st layer of the 1st layer of the 4th-layer wiring grid 404 of the direction of 135-degree slant is formed in these upper layers to 401 to 401 with the 3rd-layer wiring grid 403 of the direction of 45-degree slant.
[0011] However, the multilayer-interconnection technique of this conventional technique in which wiring of the direction of slant was used had the following troubles.
[0012] (1) With the conventional multilayer-interconnection structure, since the wiring grid of the direction of slant was prepared simply, there was a problem that the lattice point shifted. That is, as shown in drawing 29 , the 1st layer of the 2nd layer of the lattice point of 402 is set to 501 to 401. On the other hand, the 3rd layer of the 4th layer of the lattice point of 404 is set to 502 to 403. Here, when putting the 4th layer (beer hall) of the 3rd layer of a connection hole on 403 from 404, it will place at the lattice point 502. On the other hand, when putting the 3rd layer of the 2nd layer of a beer hall on 402 from 403, it will place at the lattice point 501. However, a beer hall cannot be placed if these lattice points 502 and 501 are approaching. For this reason, it will be necessary to establish a beer hall in another location. Thus, the wiring design was complicated when the lattice point shifted among the hierarchies of the upper slanting wiring grid (it is [403 and] 404 the 4th layer the 3rd layer) and a lower layer X-Y wiring grid (it is [401 and] 402 the 2nd layer the 1st layer).
[0013] (2) Resistance of the upper slanting wiring layer becomes being the same as that of a lower layer wiring layer. For this reason, even if it uses a slanting wiring layer for the upper layer, RC delay resulting from wiring is not reduced. Here, RC delay is delay by the resistance component R and the capacity component C. For this reason, even if it uses the upper slanting wiring grid, wiring structure suitable for global wiring for connecting a long distance cannot be built.
[0014] (3) Generally about the wiring pitch of the upper slanting wiring layer, it does not have a large pitch from the minimum design rule. For this reason, it does not have composition which mitigates the wiring capacity which adjoins even if it arranges a slanting wiring layer in the upper layer. The 2nd technique in which a limit of arrangement wiring spacing by the design rule arranges wiring of the severest layer aslant to the wiring grid on CAD is indicated by JP,7-86414,A" semiconductor device" about this point. However, since this conventional technique is not the configuration of taking large wiring width of face to coincidence, it cannot mitigate the above-mentioned wiring resistance. Moreover, since coupling capacity with contiguity wiring is not mitigated, RC delay of wiring is unmitigable.
[0015] (4) The configuration of a beer hall was defined as the rectangle configuration with the conventional technique. However, when connecting wiring other than wiring which intersect perpendicularly (i.e., when connecting wiring which crosses aslant), required sufficient cut area cannot be secured in a rectangular beer hall configuration. Therefore, the resistance over the electromigration phenomenon which causes a poor open circuit of wiring was inadequate.
[0016] (5) The relation of the definition of a cel low and the definition of a slanting wiring grid which arrange a logic cell to seriate and are formed was not clear. for this reason -- for example, when a total of four wiring layers of the two wiring layers and two slanting wiring layers which intersect perpendicularly were defined, it was clear that the wiring resources located in a cel low and parallel run short. Two wiring layers of the direction of slant are defined about this point on three wiring layers

which intersect perpendicularly, and the technique which solves the problem that the above-mentioned wiring resource is insufficient is indicated by JP,5-243379,A" semiconductor integrated circuit equipment." However, with this technique, the wiring layer of five layers is needed and there is a problem of causing the rise of cost.

[0017] (6) The cross talk noise which causes malfunction of a circuit was not able to be reduced within the same wiring layer. In the wiring structure equipped with the slanting wiring grid of the conventional technique, an up-and-down wiring layer does not lap in the same wiring direction. For this reason, since the coupling capacity during wiring of an up-and-down wiring layer becomes small, the problem of the cross talk noise during vertical wiring is solved. However, within the same wiring layer, since different wiring is arranged in parallel, the coupling capacity during contiguity wiring is unmitigable. That is, with the conventional slanting wiring grid technique, the cross talk noise which is between two wiring which is parallel within the same wiring layer, and is produced was unremovable.

[0018] (7) The conventional slanting wiring grid was inadequate for considering as wiring for current supply. For example, when it constitutes a pad in the core region of the chip which constitutes a combinational circuit, it is possible to use a part of this pad for current supply. (In addition, the boundary region which arranges I/O of a chip is called an I/O field to this core region.) The upper slanting wiring latticed layer can be used as auxiliary wiring for current supply in this case. In such a configuration, the conventional slanting wiring grids structure has become with structure with a wiring pitch unsuitable for constituting broad wiring, or wiring width of face. For this reason, it was the structure of not being suitable for using the upper slanting wiring latticed layer effectively as an object for current supply.

[0019] (8) Since the wire length of wiring which supplies a clock to the flip-flop in a chip from PLL (Phase Locked Loop) was long, delay was increasing.

[0020] In order that PLL may not worsen the property of the analog circuit built in a chip, it is usually arranged at the corner of a chip and is wired from this corner to each flip-flop. For this reason, wiring of die length also with the shortest near the semicircle enclosure length of a chip needed to be drawn. Therefore, while delay increased, when the number of stages of a buffer increased, the bad influence was in the duty ratio of a clock.

[0021] (9) In the case of memory circuits, such as SRAM, wiring which passes through these memory circuit top starts the coupling noise between wiring in memory, and passage wiring, and worsens the engine performance. For this reason, passage wiring on this memory circuit was avoided conventionally, and the wiring design was made. There is a conventional technique which shields passage wiring on this memory circuit. However, with this technique, in order to shield wiring, one more layer is needed further. Therefore, the configuration of a circuit was complicated. Moreover, there are other conventional techniques which use passage wiring on a memory circuit for small-size width-of-face signals. However, with this technique, the integrated circuit used as the candidate for application was limited.

[0022]

[Problem(s) to be Solved by the Invention] This invention is made in order to solve the above-mentioned trouble of the conventional technique.

[0023] and the wiring grid to which the purpose intersects perpendicularly in the direction of X-Y -- in addition, in the semiconductor integrated circuit using the multilayer-interconnection structure which prepared the wiring grid which intersects perpendicularly in the direction of slant, by utilizing a slanting wiring layer, while raising the delay characteristics and noise resistance of a circuit, it is in offering the semiconductor integrated circuit and the semiconductor integrated circuit wiring approach which enabled easy-izing of a wiring design, and reduction-ization of a manufacturing cost.

[0024]

[Means for Solving the Problem] With wiring of m (m>=2) layer with which the description of this invention is formed in the upper layer of the semiconductor region in which two or more unit element children were formed, and said semiconductor region, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually With the m+1st-layer wiring and the m+2nd-layer wiring which are located in the criteria wiring layer which forms the criteria wiring grid of the direction of X-

Y, and the upper layer of said criteria wiring layer, and intersect perpendicularly mutually The slanting wiring layer which forms the slanting wiring grid which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring grid is provided. Said slanting wiring layer While being set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring The wiring width of face of the m+1st-layer wiring and said m+2nd-layer wiring is in the point of offering the semiconductor integrated circuit equipment characterized by being set up root2 twice to the wiring width of face of each layer of said criteria wiring layer.

[0025] Moreover, as for said slanting wiring layer, the wiring thickness has other descriptions of this invention in the point set up root2 twice of the wiring thickness of said criteria wiring grid.

[0026] Moreover, as for said criteria wiring layer and said slanting wiring layer, other descriptions of this invention constitute a wiring channel field, and said wiring channel field is in the point established in the direction parallel to the cel low which has arranged to seriate the logic cell which consists of said unit element child.

[0027] Moreover, in other descriptions of this invention, wiring of said criteria wiring layer and wiring of said slanting wiring layer establish the beer hall for wiring connection in these crossover parts, and said beer hall is in the point that the cross section is the configuration of either a hexagon, an octagon and a parallelogram.

[0028] Moreover, as for said two or more unit element children, other descriptions of this invention constitute a cel, and said cel is in the point of having the obstruction field which is defined by the configuration where it met in the wiring direction of said slanting wiring grid and where wiring is not performed.

[0029] Moreover, wiring of said slanting wiring layer has other descriptions of this invention in the point that the part is constituted as power-source wiring for current supply.

[0030] Other descriptions of this invention moreover, said two or more unit element children The cel which consists of said two or more unit element children is constituted. Said cel A clock signal is supplied by the wiring path of a tree mold. Said tree type of wiring path The 1st connection by the path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 1st and 2nd points, It is in the point constituted combining the unit wiring configuration constituted by connecting the 2nd connection by the path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 3rd and 4th points with wiring of said criteria wiring layer.

[0031] Other descriptions of this invention moreover, the above-mentioned semiconductor integrated circuit equipment the [furthermore, / which is located in the upper layer of said slanting wiring layer, and intersects perpendicularly mutually] -- with p-1 (p>=2) layer wiring and the p-th-layer wiring The up wiring layer which forms the up wiring grid which crosses at the include angle of 45 degrees or 135 degrees to said slanting wiring grid or the p-th-2nd-layer wiring is provided. Said up wiring layer While being set up root2 twice to the wiring pitch of said the p-th-2nd-layer wiring between wiring of each layer of said slanting wiring layer, the wiring pitch during wiring of each class The wiring width of face of wiring of each class is in the point set up root2 twice to the wiring width of face of wiring of each layer of said slanting wiring layer, or said the p-th-2nd-layer wiring.

[0032] Moreover, said slanting wiring layer has other descriptions of this invention in the point that global wiring covering the whole chip is wired in general.

[0033] Moreover, said criteria wiring layer has other descriptions of this invention in the point that local wiring other than said global wiring is wired.

[0034] Moreover, as for said two or more unit element children, other descriptions of this invention constitute a cel, and when direct continuation of said cel should be carried out to said global wiring, it is in the point of having the output terminal configuration in which wiring and direct continuation of said slanting wiring layer are possible.

[0035] Other descriptions of this invention moreover, the above-mentioned semiconductor integrated circuit equipment A flip-flop circuit and PLL (Phase Locked Loop) arranged at the corner of a chip are provided. Furthermore, said flip-flop circuit A clock signal is supplied by the wiring path of a tree mold.

Said tree type of wiring path It is in the point by which connection is carried out near the chip center using wiring of said slanting wiring layer from said PLL, and connection is carried out hierarchical so that RC product may be made to balance through a buffer cel to said flip-flop circuit near [said] the chip center.

[0036] Moreover, other descriptions of this invention possess the SRAM circuit where the above-mentioned semiconductor integrated circuit equipment uses wiring of said criteria wiring layer for wiring of the interior further, and said slanting wiring layer is in the point that wiring which passes through said SRAM circuit top is wired.

[0037] Moreover, said criteria wiring layer is constituted for other descriptions of this invention by three layers, and the point wired in the direction parallel to the cel low which has arranged to seriate the logic cell which consists of said unit element child has the 1st-layer wiring and the 3rd-layer wiring of said criteria wiring layer.

[0038] Moreover, said criteria wiring layer has other descriptions of this invention in the point constituted by two-layer.

[0039] With moreover, wiring of m (m>=2) layer which is the semiconductor integrated circuit wiring approach that other descriptions of this invention wire the component of a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring grid While being set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring The wiring width of face of the m+1st-layer wiring and said m+2nd-layer wiring is in the point of offering the semiconductor integrated circuit wiring approach characterized by including the step formed in order to be set up root2 twice to the wiring width of face of each layer of said criteria wiring layer.

[0040] Moreover, other descriptions of this invention are in the above-mentioned semiconductor integrated circuit wiring approach to the point containing the step which inserts the buffer cel for signal magnification in the step which extracts the wiring network which produces the delay which exceeds a predetermined time delay further out of the wiring network which said criteria wiring layer constitutes, and a location connectable with wiring of said slanting wiring layer on said extracted wiring network.

[0041] Moreover, the above-mentioned semiconductor integrated circuit wiring approach has other descriptions of this invention in the point containing the step which defines further the cel which consists of said two or more unit element children, and the step which defines the obstruction field where wiring is not performed in said cel by the configuration where it met in the wiring direction of said slanting wiring layer.

[0042] Moreover, said obstruction domain-defined step has other descriptions of this invention in the point which arranges said m+1st-layer wiring or said m+2nd-layer wiring near [the] the corner.

[0043] Moreover, further, the above-mentioned semiconductor integrated circuit wiring approach is wiring of said either of m layers of said criteria wiring layer, and other descriptions of this invention are in the point containing the step which replaces the predetermined part in the middle of one wiring of said wiring of two with wiring of said slanting wiring layer, when one wiring exerts a noise on wiring of another side among parallel wiring of two belonging to the same layer.

[0044] Moreover, the above-mentioned semiconductor integrated circuit wiring approach has other descriptions of this invention in the point containing the step which inserts a buffer cel further into the path of wiring of said slanting wiring layer used for said replacement.

[0045] With moreover, wiring of m (m>=2) layer which is the cel configuration method which, as for other descriptions of this invention, arranges a cel on a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch

during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The cel which consists of two or more unit element children It is in the point of offering the cel configuration method characterized by including the step arranged based on the predetermined cutting method using the cutline of the direction of X-Y corresponding to the wiring direction of said criteria wiring layer, and the cutline of the direction of slant corresponding to the wiring direction of said slanting wiring layer.
[0046] Other descriptions of this invention moreover, the above-mentioned semiconductor integrated circuit wiring approach Furthermore, the step which sets up the 1st path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 1st and 2nd points, The step which sets up the 2nd path formed so that it might approach each other in the wiring top of said slanting wiring grid from the 3rd and 4th points, The step which forms the unit wiring configuration constituted by connecting said the 1st path and said 2nd path with wiring of said criteria wiring layer, It is in the point which contains the step which forms the wiring path of the tree mold which supplies a clock signal in the cel which consists of said two or more unit element children combining said unit wiring configuration.
[0047] With moreover, wiring of m (m>=2) layer which is the semiconductor integrated circuit wiring approach that other descriptions of this invention wire the component of a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The step connected near the chip center using wiring of said slanting wiring layer from PLL (Phase Locked Loop) arranged at the corner of a chip, It is in the point of offering the semiconductor integrated circuit wiring approach characterized by including the step connected hierarchical so that RC product may be made balancing through a buffer cel to said flip-flop circuit in said chip near [said] the chip center.
[0048] With moreover, wiring of m (m>=2) layer which is the semiconductor integrated circuit wiring approach that other descriptions of this invention wire the component of a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, It is in the point of offering the semiconductor integrated circuit wiring approach characterized by including the step which forms the SRAM circuit which uses wiring of said criteria wiring layer for wiring of the interior, and the step which forms wiring which passes through said SRAM circuit on said slanting wiring layer.
[0049]
[Embodiment of the Invention] Hereafter, with reference to a drawing, the operation gestalt of the semiconductor integrated circuit concerning this invention and the semiconductor integrated circuit wiring approach is explained to a detail.
[0050] The operation gestalt of the 1st operation gestalt 1st in the upper layer of the criteria wiring grid of the 1st layer which intersects perpendicularly mutually, and the 2nd layer Cross at the include angle of 45 degrees or 135 degrees to this criteria wiring grid, and the slanting wiring grid formed with the 3rd-layer wiring which intersects perpendicularly mutually, and the 4th-layer wiring is prepared. While shortening a wire length by having set up the wiring pitch and wiring width of face during the 3rd-layer wiring of this slanting wiring grid, and during the 4th-layer wiring root2 twice to the wiring pitch of a criteria wiring grid, it is the operation gestalt which reduced RC delay and raised noise resistance.

[0051] Drawing 1 is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit equipment concerning the 1st operation gestalt of this invention. Drawing 2 is the top view showing an example of the wiring structure at the time of wiring based on wiring grids structure as shown in drawing 1 . Moreover, drawing 3 is the A-A sectional view of drawing 4 .
[0052] As shown in drawing 1 , as for the wiring structure of the 1st operation gestalt, the 3rd layer and 4th-layer wiring equips the wiring list of the 1st layer and the 2nd layer with the wiring grid which intersects perpendicularly mutually like the conventional technique of drawing 28 . That is, to the 1st layer, the grid is arranged so that the 3rd layer and the 4th layer may cross at 45 degrees and 135 degrees, respectively.
[0053] One in drawing 1 is the wiring grid of the 1st layer, it intersects perpendicularly with the upper layer, and the wiring grid 2 of the 2nd layer is formed. Furthermore, sequential arrangement of the 4th-layer wiring grid 4 of the direction of 135-degree slant is carried out to the 3rd-layer wiring grid 3 and the 1st-layer wiring grid 1 of the direction of 45-degree slant to the 1st-layer wiring grid 1.
[0054] Here, the 1st operation gestalt sets up more widely than between the 1st-layer wiring 1 and between the 2nd-layer wiring 2 the wiring pitch between the 4th-layer wiring 4 between the 3rd-layer wiring 3 arranged in the direction of slant, respectively. Specifically, the wiring pitch between the 3rd-layer wiring 3 and between the 4th-layer wiring 4 is set up root2 twice (root2andlambda) of the wiring pitch (lambda) between the 1st-layer wiring 1 and between the 2nd-layer wiring 2.
[0055] Thereby, it is avoidable that the lattice point shifts among the hierarchies of the upper X-Y wiring grid (it is [4 and] 4 the 4th layer the 3rd layer) and a lower layer slanting wiring grid (it is [1 and] 2 the 2nd layer the 1st layer). For this reason, it becomes possible to easy-ize a wiring design. That is, the beer hall between the 2nd layer and the 3rd layer can be established in the intersection of the grid of the 1st layer and the 2nd layer, and the adjoining grid can be used for the 1st layer or 2nd-layer wiring.
[0056] Furthermore, the 1st operation gestalt sets up more widely than the 1st-layer wiring 1 and the 2nd-layer wiring 2 the wiring width of face of the 3rd-layer wiring 3 and the 4th-layer wiring 4 arranged in the direction of slant in the wiring pitch (root2andlambda). As shown in drawing 2 , specifically, the wiring width of face of the 3rd-layer wiring 3 and the 4th-layer wiring 4 is set up root2 twice (root2andd) of the wiring width of face (d) of the 1st-layer wiring 1 and the 2nd-layer wiring 2, respectively. As mentioned above, since the wiring pitch of the 3rd layer and the 4th layer has root2 doubled, wiring spacing which p of drawing 2 shows does not have breaking a design rule. For this reason, wiring width of face can be expanded, without conflicting with a design rule.
[0057] In the example shown in drawing 3 , the 1st-layer wiring 1 is arranged perpendicularly first, and the 2nd-layer wiring 2 is arranged in the direction which intersects perpendicularly with it. On the other hand, the 3rd-layer wiring 3 and the 4th-layer wiring 4 are arranged in the direction of slant. 12 in drawing is the beer hall placed between the 1st-layer wiring 1 and the 2nd-layer wiring 2, 13 is the beer hall placed between the 2nd-layer wiring 2 and the 3rd-layer wiring 3, and further 14 is the beer hall placed between the 3rd-layer wiring 3 and the 4th-layer wiring 4.
[0058] The 1st operation gestalt has set up more thickly than the 1st-layer wiring 1 and the 2nd-layer wiring 2 the wiring thickness of the 3rd-layer wiring 3 and the 4th-layer wiring 4 arranged in the direction of slant on the assumption that the description of the above-mentioned wiring pitch and wiring width of face. As shown in drawing 3 , specifically, the wiring thickness of the 3rd-layer wiring 3 and the 4th-layer wiring 4 is set up root2 twice (root2andt) of the wiring width of face (t) of the 1st-layer wiring 1 and the 2nd-layer wiring 2, respectively. In addition, ten in drawing 3 is a semi-conductor substrate with which a transistor is formed, and 11 is an interlayer insulation film. By using the structure which made the above-mentioned wiring width of face of the 3rd layer and the 4th layer and wiring thickness the 1st layer and twice [root2] the 2nd layer, the wiring cross section of the 3rd-layer wiring and the 4th-layer wiring becomes twice the wiring cross section of the 1st-layer wiring and the 2nd-layer wiring, as shown in the following formulas.
[0059] root2xroot2=2, for this reason the wiring resistance per unit length are set to one half of the 1st layer and 2nd-layer wiring. On the other hand, although the opposed face product with contiguity wiring

becomes root2 twice, since contiguity wiring spacing also becomes root2 twice, it is the same as that of the capacity between contiguity wiring in the 1st-layer wiring and the 1st-layer wiring. [of the capacity between contiguity wiring in the 3rd-layer wiring and the 4th-layer wiring] Since the capacity between contiguity wiring has the same wiring resistance at one half, the wiring RC delay per unit length is set to one half of the 1st layer and 2nd-layer wiring. In addition, delay according [wiring RC delay] to the resistance component and capacity component of wiring is said.

[0060] As mentioned above, according to the 1st operation gestalt, the wiring pitch during the 3rd-layer wiring and during the 4th-layer wiring is set up root2 twice to the wiring pitch during the 1st-layer wiring and during the 2nd-layer wiring. For this reason, it can avoid that the lattice point shifts among the hierarchies of the upper slanting wiring grid and a lower layer criteria wiring grid, and it becomes possible to easy-ize a wiring design.

[0061] Moreover, since wiring width of face was also set up root2 twice, wiring RC delay can be reduced. Furthermore, since wiring thickness was also set up root2 twice, wiring RC delay can be reduced further and big effectiveness is acquired from a viewpoint of raising a speed of a circuit of operation by comparatively long wiring.

[0062] The operation gestalt of the 2nd operation gestalt 2nd is an operation gestalt which inserts a repeater cel (buffer cel) in wiring, and prevents generating of the timing error by wiring delay further in the multilayer-interconnection structure using the slanting wiring grid of the 1st operation gestalt.

[0063] Drawing 4 (a), (b), (c), and (d) are drawings showing the insertion procedure of the repeater cel of the 2nd operation gestalt. Drawing 5 (a) and (b) are drawings for explaining wiring delay. With reference to drawing 4 and drawing 5 , the insertion procedure of the repeater cel of the 2nd operation gestalt is explained concretely.

[0064] First, all networks are wired with wiring of only the direction of X-Y only using the 1st layer and the 2nd layer. Next, delay analysis is performed using a simulator and the network which has started the timing error is extracted. The following processings are performed to this extracted network.

[0065] That is, a repeater cel is inserted to the network which started the timing error. As an insertion location of this repeater cel, the 3rd layer and the 4th layer are used and a repeater cel is inserted in a location connectable with wiring of the direction of slant. A wire length can be shortened by using the 3rd layer or the 4th layer.

[0066] For example, the timing error should occur in a network as shown in drawing 4 (d). In this network, three kinds, drawing 4 (a), (b), and (c), can be considered as the insertion point of the repeater cel 20 between a cel 21 and a cel 22, and a direction of wiring. In the example of drawing 4 (a), after using the wiring 23 of the direction of X first and then inserting the repeater cel 20, the slanting wiring 25 is used. In the example of drawing 4 (b), after inserting the repeater cel 20 first and using the wiring 34 of the direction of slant, the wiring 35 of the direction of X is used. In the example of drawing 4 (c), after inserting the repeater cel 20 first and using the wiring 45 of the direction of X, the wiring 46 of the direction of slant is used.

[0067] A difference of the insertion point of the repeater cel of drawing 4 (a), (b), and (c) produces the difference of allocation of delay with between the repeater cel 20 and the cel 22 which carries out a signal input between the cel 21 which outputs a signal, and the repeater cel 20. When the example of drawing 4 (a) and drawing 4 (b) is compared, the delay between a cel 21 and the repeater cel 20 has less drawing 4 (b) than the example of drawing 4 (a). On the other hand, the delay between the repeater cel 20 and a cel 22 has less drawing 4 (a) than the example of drawing 4 (b). It is dependent on the transistor size of a cel 21 and the repeater cel 20 which example can make actual delay small. Therefore, it is necessary to analyze delay in all the combination that can be considered generally, and to determine the operation of the insertion point of a final repeater, and the wiring direction. However, in the example of drawing 4 (c), delay becomes large compared with other examples clearly.

[0068] About wiring width of face, if the wiring delay formula of ERUMOA is followed, as for wiring delay, the direction gradually made thin from the cel which carries out the signal output of the wiring width of face will become short. That is, wiring delay becomes [using the thick wiring width of face 74 rather than / as those who continued using the first thick wiring width of face 63 as shown in drawing 5

(a), and used the thin wiring width of face 64 show drawing 5 (b), continue using the first thin wiring 73, and] short.
[0069] wiring with which wiring of the direction of slant met X and a Y-axis -- root -- since it is thick twice, wiring delay becomes short rather than the case where the direction at the time of having used wiring of the direction of slant first, and using wiring of X or the direction of Y continuously continues first using wiring of X or the direction of Y, and uses wiring of the direction of slant. That is, it is understood from the example of drawing 4 (c) that, as for wiring delay, the direction of the example of drawing 4 (b) becomes short.
[0070] Therefore, the Ruhr at the time of inserting a repeater cel by the case where slanting wiring is used is specified as follows.
[0071] (1) Connect slanting wiring to wiring near the output terminal of a signal.
(2) Connect slanting wiring to the output terminal of a signal.
(3) Use slanting wiring abundantly to wiring near the signal output terminal of a repeater cel.
(4) Connect wiring of the direction of slant to the signal output terminal of a repeater cel.
(5) Arrange a repeater cel in the location which can connect slanting wiring to a signal output terminal.
[0072] If the above Ruhr is followed, the structure of a repeater cel will also be specified as follows.
[0073] (1) Form a signal input terminal so that it may become easy to connect with wiring which met in the direction of X-Y. That is, a signal input terminal is made to the 1st layer.
(2) Further, a signal output terminal is formed so that connecting with wiring of the direction of slant may become easy. That is, a signal output terminal is made to the 3rd layer.
[0074] As mentioned above, in order to prevent generating of the timing error by wiring delay, in case the repeater cel which relays and amplifies a signal is inserted on a wiring network according to the 2nd operation gestalt, a repeater cel is inserted in a location connectable with this slanting wiring grid using a slanting wiring grid. For this reason, a repeater cel can be inserted on the optimal conditions, a wire length can be shortened, and wiring delay can be reduced further.
[0075] The operation gestalt of the 3rd operation gestalt 3rd is an operation gestalt which prepares a wiring channel in the direction parallel to a cel low, and cancels the lack of a wiring resource of the direction of a cel low in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0076] Drawing 6 is the layout pattern showing the configuration of the semiconductor integrated circuit concerning the 3rd operation gestalt of this invention.
[0077] two or more cel lows which the semiconductor integrated circuit of drawing 6 arranged the logic cell to seriate, and were formed -- it has 80. two or more of these cel lows -- the multilayer interconnection which has the slanting wiring grid shown in drawing 1 is formed in the upper part of 80.

[0078] Specifically one in drawing 6 is the 1st-layer metal wiring, 2 is the 2nd-layer metal wiring, and 3 is the 3rd-layer metal wiring, and 4 is the 4th-layer metal wiring. the configuration of drawing 6 -- setting -- each -- the wiring channel 85 which consists of each metal wiring 1, 2, 3, and 4, respectively is formed in the direction parallel to cel low 80. namely, a cel low -- the wiring channel 85 is formed in the direction parallel to 80. For this reason, the wiring resource of the direction of a cel low which requires more wiring resources is securable with few wiring hierarchies.
[0079] As mentioned above, according to the 3rd operation gestalt, by few wiring hierarchies, the lack of a wiring resource of the direction of a cel low which requires more wiring resources can be canceled, and a wiring resource can be secured.
[0080] In the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt, the operation gestalt of the 4th operation gestalt 4th is an operation gestalt which improved the configuration so that the cut area of the beer hall which connects wiring which crosses aslant may not become inadequate.
[0081] Drawing 7 (a), (b), (c), and (d) are the part plans showing the configuration of the beer hall of the semiconductor integrated circuit concerning the 4th operation gestalt, respectively.
[0082] In the multilayer-interconnection structure of having the slanting wiring grid which showed the

semiconductor integrated circuit concerning the 4th operation gestalt to drawing 1 When the direction wiring of X-Y (the 1st layer or the 2nd layer) and the direction wiring of slant (the 3rd layer or the 4th layer) which accomplishes the include angle of 45 degrees or 135 degrees to this are connected As shown in drawing 7 (a), (b), (c), and (d), The longitudinal section uses the beer hall of an octagon, a parallelogram, or a hexagon. By using the beer hall of these cross-section configurations, the beer hall cut of sufficient cross-sectional area required between the crossing wiring layers can be created.

[0083] Beer hall 90A of an octagon is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (a). Moreover, beer hall 90B of a parallelogram is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (b).

[0084] In addition, it is possible that beer halls approach unusually with the example shown in drawing 7 (b). In order to avoid this, the configuration of the hexagon shown in drawing 7 (c) and drawing 7 (d) is offered. Beer hall 90C of a hexagon is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (c). Moreover, beer hall 90D of a hexagon is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (d).

[0085] As mentioned above, according to the 4th operation gestalt, let the cross-section configuration of a beer hall of connecting wiring which crosses aslant be an octagon, a parallelogram, or a hexagon. For this reason, the cut area of the beer hall which connects wiring which crosses aslant is fully secured. The operation gestalt of the 5th operation gestalt 5th is an operation gestalt which defines the obstruction field of wiring the optimal in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.

[0086] Drawing 8 (a) and (b) are drawings showing the cel or mega cell in the semiconductor integrated circuit concerning the 5th operation gestalt of this invention.

[0087] 101 shown in drawing 8 (a) is the cel in which two or more unit element children were formed, or the mega cell which carried out two or more sets of these cels. This cel or mega cell 101 is divided into the service area 102 and the transistor field 103 bordering on 45-degree Rhine 101a of those four corners. In the transistor field 103, a transistor and low order hierarchy cel 103a are arranged. On the other hand, it is prepared in a service area 102 in order to use effectively the four corners of a cel (are mentioned later) for the purpose of easing the wiring confusion produced near [four-corners] a cel, and neither a transistor nor a low order hierarchy cel is arranged. In addition, a cel is explained as a thing containing the above-mentioned mega cell below.

[0088] furthermore, as shown in drawing 8 (b), especially wiring arranged to the transistor field 103 of the above-mentioned cel 101 was mentioned above near the four-corners Rhine 101a -- it is good to use 45 degrees of 135-degree slanting wiring 113 again.

[0089] Thus, in case a cel or a mega cell is designed, the form where slanting wiring (45 degrees or 135 degrees) was met can define the obstruction of wiring by preparing the above-mentioned service area and making it the configuration which does not use the four corners. Next, this point is explained.

[0090] Drawing 9 (a) and (b) are drawings showing the example of the obstruction of wiring concerning the 5th operation gestalt. In the example shown in drawing 9 (a), the obstruction field in a cel 101 is made the definition by the set of the small rectangle 122. Here, an obstruction field is a field for defining the obstruction of wiring in a wiring design.

[0091] The example shown in drawing 9 (b) defines the obstruction field in a cel 101 by the polygon or its set. namely, the case where there are two obstruction fields in the example of drawing 9 (b) -- them -- a trapezoid -- it defines as 132,133, respectively.

[0092] Although there is a difficulty that the amount of data in a CAD design increases, in the example shown in drawing 9 (a), the example shown in drawing 9 (b) to this can define an obstruction field by the small amount of data.

[0093] Drawing 10 (a) and (b) are drawings showing the effectiveness of the 5th operation gestalt.

[0094] In the usual X-Y wiring grid model, as shown in drawing 10 (a), the obstruction field 142 of the cel or mega cell 141 interior is defined as a set of a rectangular rectangle. When rectangular wiring was

performed using these cels or mega cells 141, there was a problem that the degree of integration of a chip fell owing to the increase of the congestion factor of the wiring 143 in the four-corners neighborhood 144 and it.

[0095] On the other hand, if it wires using the cel and mega cell 101 which were created by the technique of the 5th operation gestalt mentioned above, as shown in drawing 10 (b), the obstruction field 152 is defined by the configuration which does not use the four corners of a cel or a mega cell. The configuration where slanting wiring was met can define this obstruction field 152. For this reason, the congestion factor of the wiring 153 in the above-mentioned four-corners neighborhood 154 is eased, and the degree of integration of a chip improves.

[0096] As mentioned above, according to the 5th operation gestalt, an obstruction field is defined in the design of a cel or a mega cell by the configuration where slanting wiring was met with the configuration which does not use the four corners of a cel or a mega cell. For this reason, the four corners of a cel can be used effectively. Moreover, the congestion factor of wiring in the above-mentioned four-corners neighborhood is eased, and the degree of integration of a chip improves.

[0097] The operation gestalt of the 6th operation gestalt 6th is an operation gestalt which controls the cross talk noise produced when there is wiring arranged in parallel in this layer in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.

[0098] Drawing 11 (a), (b), and (c) are drawings showing the important section of the configuration of the semiconductor integrated circuit concerning the 6th operation gestalt of this invention. In addition, the same sign is given to drawing 6 and a common element, and the explanation is omitted.

[0099] The case where there is wiring 161,162 arranged by being parallel in this layer as shown in drawing 11 (a) is considered. the 6th operation gestalt -- one of the wiring (for example, wiring 162) -- on the way -- a wiring layer is changed so that a part may be replaced with the direction wiring 173,174 of slant which accomplishes the include angle of this wiring 162, 45 degrees, or 135 degrees, as shown in drawing 11 (b). By replacement of this wiring, the distance to which two wiring of this layer becomes parallel becomes short, and can control generating of a cross talk noise.

[0100] Moreover, if the direction which receives a noise for the direction which generates a noise among the parallel wiring 161,162 with wiring 161 is assumed to be wiring 162, in case wiring 162 will be changed with the direction wiring 173,174 of slant mentioned above, one or more buffer cels 183 are inserted on the direction wiring 173,174 of slant.

[0101] Thus, it is possible by inserting a buffer cel into the path of the direction wiring of slant to prevent propagation of a noise completely. For example, if **** distance is restricted so that the voltage level of a cross talk noise produced between two wiring arranged in parallel in this layer may not exceed the logic threshold of said buffer cel 183 inserted as an object for noise cancellation, it is possible to control a noise completely.

[0102] As mentioned above, according to the 6th operation gestalt, in the middle of wiring of one of wiring arranged by being parallel in this layer, a wiring layer is changed so that a part may be replaced with the direction wiring of slant. Moreover, a buffer cel is inserted into the path of the direction wiring of slant used for replacement. For this reason, the distance to which two wiring in the same layer becomes parallel becomes short, and generating of the cross talk noise during wiring is controlled.

[0103] The operation gestalt of the 7th operation gestalt 7th is an operation gestalt using the wiring resource of a slanting wiring grid as an object for current supply in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.

[0104] Drawing 12 is drawing showing the important section configuration of the semiconductor integrated circuit concerning the 7th operation gestalt of this invention. The same sign is given to drawing 6 and a common element, and the explanation is omitted.

[0105] As shown in drawing 12 , some of 3rd-layer wiring 3 located in the upper layer of the 1st-layer wiring 1 and the 2nd-layer wiring 2 and 4th-layer wiring 4 are used for the wiring 191 for current supply for current supply. thereby -- the wiring resource of the common signal line of the direction of slant -- a part -- as the object for current supply -- using -- a cel low -- the power source which run short by 80 is suppliable.

[0106] As mentioned above, according to the 7th operation gestalt, a part of wiring resource of the general signal point of the direction of slant is used as wiring for current supply. For this reason, the power source which run short in a cel low is suppliable.
[0107] The operation gestalt of the 8th operation gestalt 8th is an operation gestalt which optimizes arrangement of a cel in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0108] Drawing 13 (a) and (b) are drawings showing the arrangement technique of the cel of the semiconductor integrated circuit concerning the 8th operation gestalt of this invention.
[0109] Usually, in the LSI design by CAD, the configuration method of a cel is performed in consideration of the ease of wiring so that a wire length may become short. The technique of the following which used the top-down technique is used for the activity of arranging which cel where, in that case.
[0110] By this conventional technique, as shown in drawing 13 (b), the set of the cel which it is going to arrange from now on is first divided into two by the cutline 260 in every direction. Next, a cel 201,210 is arranged so that the number of wiring which crosses this cutline 260 may decrease. This two piece housing is repeated until it halves after that still more nearly similarly using a cutline and all fields become the minimum unit. The above-mentioned conventional technique is called the mini cutting method.
[0111] Here, the conventional cutline 260 is the straight line of length and width corresponding to the wiring grid of the direction of X-Y, as shown in drawing 1313 (b). However, if the direction wiring of slant mentioned above is prepared, what has the include angle of 45 degrees as an obstruction of wiring as the 5th operation gestalt explained will appear. For this reason, the location of the optimal cel is no longer obtained only by the cutline 260 of length and width.
[0112] Then, as shown in drawing 13 (a), in addition to the cutline which intersects perpendicularly in all directions [conventional], the cutline 250 of the direction of slant is used for the 8th operation gestalt. A cel 201,210 is arranged so that the number of wiring which crosses the cutline 250 of this direction of slant may become min. The location of a cel can be decided to be able to perform optimal wiring in every direction and the direction of slant by this, and it becomes possible to raise the degree of integration of LSI.
[0113] As mentioned above, according to the 8th operation gestalt, in case arrangement of the cel in an LSI design is designed, cel arrangement is performed by the mini cutting method for using the cutline of the direction of slant. For this reason, the location of a cel can be optimized so that optimal wiring can be performed in the multilayer-interconnection structure using a slanting wiring grid. Therefore, the degree of integration of LSI can be raised.
[0114] The operation gestalt of the 9th operation gestalt 9th is an operation gestalt which optimizes the configuration of the clock tree in the wiring design for the clock supply in the case of using the direction wiring of slant, and reduces dispersion in wiring RC delay in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0115] Drawing 14 (a), (b), (c), and (d) are drawings for explaining the basic configuration of the clock tree of the semiconductor integrated circuit equipment concerning the 9th operation gestalt of this invention.
[0116] In order to have the delay of a clock signal for every path pass, generally the wiring configuration of a tree mold is used. In this case, if only the direction of X-Y is the multilayer-interconnection structure of a wiring grid, as shown in general in drawing 14 (d), it will become the repeat of the wiring configuration of H mold shown in drawing 1414 (b).
[0117] In construction of such a tree wiring path, the 9th operation gestalt takes the repeat structure of the configuration where the direction wiring of slant as shown in drawing 14 (a) was utilized, as shown in drawing 14 (c). That is, as shown in drawing 14 (a), a path is connected so that it may approach each other using a slanting wiring grid from four points P1, P2, P3, and P4. in every direction at the points P5 and P6 where two points, P1, P2, and P3 and P4, were formed at a time -- the configuration of drawing 14 (a) is acquired by connecting with wiring of one of wiring layers. However, let the points P5 and P6

where a path branches be the locations to which the delay of the downstream of signal propagation is equal.
[0118] Although a wire length has only several% of difference when the wiring configuration of the conventional H mold shown in drawing 14 (b) is compared with the wiring configuration of the 9th operation gestalt shown in drawing 14 (a), there is a dominance difference in wiring RC delay. Temporarily, the wiring resistance r and the wiring capacity c per unit length of each wiring layer presuppose that it is equal, and suppose that volume load is not attached to an end. Here, the wiring delay DH of the wiring configuration of the conventional H mold shown in drawing 14 (b) is obtained by the following formulas.
[0119]
DH=rl(2cl)+1/2 rl-cl=2.5rcl2 (1)
(However, let l be the die length of wiring in drawing 14)
On the other hand, the wiring delay Dd of the wiring configuration of the 9th operation gestalt shown in drawing 14 (a) is obtained by the following formulas.
[0120]
Dd=1/2r (root2l.) and c(root2l.) =rcl2 (2)
In addition, since it is minute, the distance between P5 and P6 of drawing 14 (a) can be disregarded on count of (2).
[0121] Therefore, in the configuration of the 9th operation gestalt of drawing 14 (a), only the following parts can make RC delay smaller than H mold of drawing 14 (b).
[0122]
DH-Dd=(2.5-1)rcl2=1.5rcl2 (3)
Reduction of this RC delay is effectiveness acquired when wiring branching becomes the upper approach of signal propagation. Moreover, the reduction effectiveness of this delay will become still larger if load-carrying capacity is attached to the downstream. Furthermore, generally, since it is smaller than wiring resistance of the direction wiring of X-Y, the direction of wiring resistance of the direction wiring of slant to be used becomes the factor which increases the reduction effectiveness of delay.
[0123] In addition, when a clock terminal is distributed over an ununiformity, the balance point of delay may be unable to be taken on Rhine of drawing 14 (a). A wiring configuration is corrected as shown in drawing 15 in such a case. With the wiring configuration of this drawing 15 R> 5, the balance point can be set up exactly. What is necessary is just to use the wiring configuration of this drawing 15 partially in the clock tree of whole drawing 14 (c).
[0124] Moreover, as shown in drawing 16 (b), in order to arrange other buffers and delay in near the output terminal of the buffer 310 inserted in the middle of the tree, an alternate route 311 may be established. The number of beer halls is reducible by using the direction wiring of slant as shown in drawing 16 (a) in such a case. Therefore, the effectiveness in respect of reduction of beer hall resistance and electromigration resistance with the advantageous configuration of this drawing 16 (a) is acquired.
[0125] In addition, the example of the wiring design using a maze running method is shown as the concrete wiring approach in case automatic wiring performs the slanting wiring grid of 45 degrees and the direction of 135 degree to drawing 17 (a), (b), and (c).
[0126] 320,321 in drawing 17 (a), (b), and (c) is the starting point and the terminal point of a terminal pair which should be connected mutually. 330 is a wiring keepout area in a chip core region. Wiring is arranged in the path shown from the starting point 320 to a terminal point 321 by the thick wire in drawing 17 (a), (b), and (c). The example shown in drawing 17 (a) shows wiring at the time of using together the direction wiring of X-Y, and the direction wiring of slant. The example of drawing 17 (b) shows the example which wired only with the direction wiring of slant. Moreover, the example drawing 17 R> 7 (c) shown shows wiring at the time of using the direction wiring of X-Y, and slanting wiring of the direction of 135 degree.
[0127] As mentioned above, according to the 9th operation gestalt, in construction of a tree path, the configuration which combined the unit wiring configuration where the direction wiring of slant was utilized is used. For this reason, wiring RC delay is reduced and the optimal clock tree can be built.

[0128] In the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt, the operation gestalt of the 10th operation gestalt 10th is constituting the wiring grid of the direction of X-Y of drawing 3 by the wiring layer of three layers which intersects perpendicularly mutually, and is an operation gestalt to which the wiring resource of the direction of a cel low is made to increase.
[0129] Drawing 18 is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit concerning the 10th operation gestalt of this invention. Drawing 19 is the sectional view which observed the wiring structure at the time of wiring based on wiring grids structure as shown in drawing 18 from X shaft orientations of drawing 18 .
[0130] In drawing 18 , the wiring grid of the direction of X-Y is constituted by wiring of three layers. specifically, it is shown in drawing 1818 -- as -- the 1st -- layer 601 -- the 2nd layer of 602 and the wiring grid to which wiring of 603 and the 3rd layer of the 4th layer of 604 and the 5th-layer wiring 605 cross at right angles mutually are constituted. Here, the 10th operation gestalt offers the 3rd-layer wiring 603 which is parallel to the 1st-layer wiring 601. That is, to the 1st layer and the 3rd-layer wiring, the grid is arranged so that the 4th-layer wiring and the 5th-layer wiring may cross at 45 degrees and 135 degrees, respectively.
[0131] 601 in drawing 18 is the wiring grid of the 1st layer, it intersects perpendicularly with the upper layer, and the wiring grid 602 of the 2nd layer is formed. It intersects perpendicularly with the upper layer of this 2nd wiring grid 602, and the 3rd wiring grid 603 is formed. Furthermore, sequential arrangement of the 5th-layer wiring grid 605 of the direction of 135-degree slant is carried out to the 4th-layer wiring grid 604, and the 1st-layer wiring grid 601 and the 3rd-layer wiring grid 603 of the direction of 45-degree slant to the 1st-layer wiring grid 601 and the 3rd-layer wiring grid 603.
[0132] The 10th operation gestalt sets up the wiring pitch between the 5th-layer wiring 605 root2 twice (root2andlambda) of the wiring pitch (lambda) between the 2nd-layer wiring 602 and the 3rd-layer wiring 603 like the 1st operation gestalt between the 4th-layer wiring 604 arranged in the direction of slant during the 1st-layer wiring 601 and during the 2nd-layer wiring 602, respectively. Moreover, as shown in drawing 19 , the wiring width of face between the 5th-layer wiring 605 is set up root2 twice (root2andt) of the wiring pitch between the 2nd-layer wiring 602 and the 3rd-layer wiring 603 (t) between the 4th-layer wiring 604 arranged in the direction of slant during the 1st-layer wiring 601 and during the 2nd-layer wiring 602, respectively. In addition, as for the 1st-layer wiring 601, the 2nd-layer wiring 602, and the 3rd-layer wiring 603, it is desirable to define as the minimum wiring width of face which becomes settled by the design rule in a wiring design, height, and a wiring pitch.
[0133] Return, the 1st-layer wiring 601, and the 3rd-layer wiring 603 are formed in the direction parallel to the direction of a cel low at drawing 18 . For this reason, the wiring resource of the direction of a cel low can be made to increase further as compared with the 1st operation gestalt. In addition, the 10th operation gestalt is different from the 3rd operation gestalt in the point of not preparing a wiring channel.
[0134] In the multilayer structure in the wiring grid which intersects perpendicularly in the conventional direction of X-Y, when wiring of two or more layers was formed in parallel, the cross talk noise by parallel arrangement of wiring was produced. The 10th operation gestalt can secure the wiring resource of the direction of a cel low by combining parallel arrangement of a slanting wiring grid and wiring, controlling generating of a cross talk noise.
[0135] As mentioned above, according to the 10th operation gestalt, the 1st-layer wiring and the 3rd-layer wiring are formed in the direction parallel to a cel low, and the above-mentioned slanting wiring grid is formed in this upper layer. For this reason, the wiring resource of the direction of a cel low is securable.
[0136] In addition, the wiring grid of one layer or two or more layers may be formed in the pan of the slanting wiring grid which the 4th-layer wiring 604 and the 5th-layer wiring 605 accomplish as a modification of the 10th operation gestalt at the upper layer. To the 5th-layer wiring 605, the upper wiring grid is formed at the include angle whose two wiring grid pairs which the 6th-layer wiring and the 7th-layer wiring which intersect perpendicularly mutually make are 45 degrees, henceforth, repeats

this configuration to this pan, and is constituted. That is, in addition to the criteria wiring grid which the 1st-layer wiring, the 2nd-layer above-mentioned wiring, and the 3rd-layer above-mentioned wiring make, and the slanting wiring grid which the 4th-layer wiring and the 5th-layer wiring make, two wiring grid pairs which intersect perpendicularly still more nearly mutually, the p-1st layer and the p-th layer, are the p-th. - The wiring structure of q layers which makes the include angle of 45 degrees and formed to two-layer wiring be offered. (However, q>=5)
Here, the p-1st layer and p-th-layer wiring which intersects perpendicularly mutually is set up root2 twice of the wiring pitch of the p-th-2nd-layer wiring. Moreover, the wiring width of face of the p-1st layer and p-th-layer wiring is set up root2 twice of the wiring pitch of the p-th-2nd-layer wiring, respectively. In addition, as for the 1st-layer wiring, the 2nd-layer wiring, and the 3rd-layer wiring, it is desirable to define as the minimum wiring width of face which becomes settled by the design rule in a wiring design, height, and a wiring pitch.
[0137] According to this modification, while raising the degree of integration of a circuit, wiring RC delay can be reduced.
[0138] The operation gestalt of the 11th operation gestalt 11th is an operation gestalt which raises circuit speed in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt by using wiring of the wiring layer which makes a slanting wiring grid for global wiring which is comparatively long wiring.
[0139] Drawing 20 is drawing explaining arrangement of wiring in the 11th operation gestalt. Drawing 21 is drawing explaining global wiring in the 11th operation gestalt. In addition, although the case where the wiring grid of the direction of X-Y is formed with the 1st-layer wiring, the 2nd-layer wiring, and the 3rd-layer wiring, and a slanting wiring grid is formed with the 4th-layer wiring and the 5th-layer wiring like the 10th operation gestalt for the facilities of an understanding is explained as an example below It cannot be overemphasized that it can apply also when the wiring grid of the direction of X-Y is formed with the 1st-layer wiring and the 2nd-layer wiring with which this is shown in the 1st operation gestalt.
[0140] As shown in drawing 20 , the upper wiring of the 4th-layer wiring with which the 11th operation gestalt makes a slanting wiring grid, and the 5th-layer wiring is used for global wiring. In global wiring, in order that the delay characteristics generally called for may be critical and these delay characteristics may influence the circuit speed of the whole chip, especially wiring RC delay poses a problem. Here, as for the above-mentioned operation gestalt, RC delay of the upper wiring is set to one half to lower layer wiring (wiring of the direction of X-Y). For this reason, a speed of a circuit of operation can be raised by using for global wiring wiring of the slanting wiring grid which is this upper wiring. On the other hand, as for lower layer wiring (wiring of the direction of X-Y), being used for local wiring is desirable.
[0141] In addition, global wiring is wiring used for the clock network (clock wiring) and bus covering the whole chip, a power-source reinforcement wire, etc. here. For example, if wiring distance considers wiring of about 2.5mm or more as global wiring in the case of a 0.25-micrometer design rule, wiring RC delay will be set to about 1.4ns in this case. On the other hand, local wiring means short wiring of wiring distance from this.
[0142] In addition, the wiring pitch of wiring (lower layer wiring) of the direction of X-Y used for this local wiring becomes narrower than the wiring pitch of the direction wiring of slant (the upper wiring). In this case, as shown in drawing 2121 , as for the cels 610 with the strong drive force, such as a clock buffer cel and a buffer cel for buses, it is desirable to carry out direct continuation to global wiring without wiring (601-604) of each class the degree of capital. For this reason, the 11th operation gestalt makes the configuration of the output terminal of a cel with the strong drive force directly the configuration in which wiring of the slanting wiring grid of the 4th more than layer and connection are possible. As shown in drawing 22 , the output terminal 704 of a cel with these strong drive force is defined as the access point where the upper slanting wiring grid intersects perpendicularly.
[0143] By making the output terminal configuration of these cels into the configuration which can carry out direct continuation to global wiring, the wire length about these cels is shortened and a wiring design also becomes easy. Moreover, since it connects with wiring of the slanting wiring grid of the 4th more than layer of the direct upper layer, the number of beer halls can be reduced and resistance resulting

from a beer hall can be reduced.
[0144] As mentioned above, according to the 11th operation gestalt, wiring of the wiring layer which makes a slanting wiring grid is used for global wiring which is comparatively long wiring. For this reason, wiring RC delay of wiring which influences a circuit property greatly is reduced, and circuit speed improves. The operation gestalt of the 12th operation gestalt 12th is an operation gestalt which makes RC product balance in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt by wiring a chip pin center,large using a slanting wiring grid from PLL in the structure of clock wiring for the clock supply from a PLL (Phase Locked Loop) circuit, and defining wiring to each flip-flop from this chip pin center,large by the tree structure.
[0145] Drawing 23 (a) is drawing showing the wiring technique of clock supply wiring from the conventional PLL. Since PLL803 is a sensitive analog cel, it is necessary to arrange it at the edge of a chip on a circuit property. For this reason, by the conventional technique using the wiring 801 of the direction of X-Y, the wire length was long. Drawing 23 (b) is drawing showing the wiring technique of clock supply wiring from PLL of the 12th operation gestalt. The 12th operation gestalt performs clock supply wiring 802 in the chip pin center,large 804 from PLL802 using a slanting wiring grid. For this reason, while a wire length is shortened, wiring RC delay is reduced. As shown in drawing 24 , wiring to the cluster which each flip-flop makes from this chip pin center,large is made through a buffer cel. Drawing 25 is drawing showing the clock tree of the 12th operation gestalt. As shown in drawing 24 , a clock wiring path consists of each buffer cel so that RC product may be made to balance. That is, a clock wiring path consists of chip pin center,larges hierarchical so that delay of the direction of X-Y and the direction of slant may be made to balance. This hierarchical clock tree may be constituted like the 9th above-mentioned operation gestalt, as shown in drawing 26 . In addition, PLL may be transposed to DLL.
[0146] In addition, it is better to set wiring width of face to these clock wiring paths widely, using the upper slanting wiring grid preferentially. That is, if the wiring pitch of a slanting wiring grid is twice [root2] the lower layer X-Y wiring grid, it is easy for a slanting wiring grid to use thick wiring width of face, and the increment in the wiring RC delay accompanying the fall of the wiring resistance R can be suppressed by this.
[0147] As mentioned above, according to the 12th operation gestalt, a slanting wiring grid is used for clock supply wiring in the chip pin center,large from PLL, and in clock supply wiring to each flip-flop on a chip from this chip pin center,large, a clock wiring path is constituted hierarchical so that delay of the direction of X-Y and the direction of slant may be made to balance. For this reason, while the wire length for clock supply is shortened, wiring RC delay is reduced.
[0148] In the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt, the operation gestalt of the 13th operation gestalt 13th is an operation gestalt which the slanting wiring grid was used [gestalt] and carried out passage wiring of this SRAM top, when SRAM is arranged on a chip. In addition, in the 13th operation gestalt, SRAM may be transposed to DRAM and may be constituted.
[0149] Drawing 27 is drawing explaining passage wiring on the memory in the 13th operation gestalt. The wiring layers 1 and 2 of the lower layer direction of X-Y are used for a word line and a bit line, and are formed in the SRAM901 interior. On the other hand, the passage wiring 3 and 4 is wired using the upper slanting wiring grid. That is, the wiring 1 and 2 of the direction of X-Y of the SRAM901 interior and the passage wiring 2 and 3 using a slanting wiring grid do not become parallel like before. For this reason, a coupling noise is reduced as compared with the former.
[0150] As mentioned above, using a slanting wiring grid, to wiring in memory, the crossed axes angle of 45 degrees or 135 degrees is accomplished, and, according to the 13th operation gestalt, passage wiring which passes through a memory top is formed. For this reason, the coupling noise of wiring in memory and passage wiring is reduced.
[0151] In addition, this invention can be variously changed in the range which is not limited to the gestalt of operation mentioned above and does not deviate from the summary.
[0152]

[Effect of the Invention] As explained above, while the delay characteristics and noise resistance of a circuit improve, according to this invention, in addition to the wiring grid which intersects perpendicularly in the direction of X-Y, easy-izing of a wiring design and reduction-ization of a manufacturing cost are realized by utilizing a slanting wiring layer in the semiconductor integrated circuit using the multilayer-interconnection structure which prepared the wiring grid which intersects perpendicularly in the direction of slant.

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TECHNICAL FIELD

[Field of the Invention] This invention relates to the semiconductor integrated circuit equipment, the semiconductor integrated circuit wiring approach, and cel configuration method which have multilayer-interconnection structure. In the semiconductor integrated circuit with which the wiring layer of the wiring grid of the direction of slant was especially formed in the upper layer of the wiring layer of the wiring grid of the direction of X-Y, it is related with the semiconductor integrated circuit and the semiconductor integrated circuit wiring technique of realizing reduction of delay of a circuit, and improvement in noise resistance.

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PRIOR ART

[Description of the Prior Art] The method which accumulates the wiring layer which intersects perpendicularly on the upper layer has been taken by the multilayer-interconnection structure of LSI by a conventional standard cell or a conventional gate array method. That is, as it says that the 1st layer and the 2nd layer intersect perpendicularly and the 2nd layer and the 3rd layer intersect perpendicularly, it is the configuration that the n-1st layer and the n-th layer intersect perpendicularly. In the multilayer-interconnection structure where such each class intersects perpendicularly, when connecting two points of the direction of a vertical angle, the point which separated by Euclidean distance will be connected. For this reason, wiring of the die length more than one twice [root2] the distance of a slant range is needed. Therefore, the multilayer-interconnection structure of a rectangular mold had produced the overhead also in delay characteristics also in degree of integration.
[0003] However, in case an LSI wiring design is carried out on a computer, the technique of wiring by the rectangular coordinate system is simple in algorithm. For this reason, on the computer, the above-mentioned overhead was disregarded and the wiring design was performed.
[0004] However, the delay component resulting from wiring structure has come to influence the performance of the whole circuit as detailed-ization of circuit structure progresses. It is impossible for this reason, to disregard the overhead by the above-mentioned wire length becoming long.
[0005] Specifically, the delay component which originates in wiring resistance the 1st occupies the great portion of critical path delay. Thus, the effect which a wire length has on circuit performance is increasing.
[0006] Moreover, the coupling capacity during wiring which adjoins rather than the capacity of an opposite substrate of the items of the load-carrying capacity which originates [2nd] in wiring is more dominant. For this reason, it is an important element for raising circuit performance how the capacity during adjoining wiring is mitigated.
[0007] Furthermore, coupling noise **** malfunction which originates in the coupling capacity during this wiring the 3rd is also aggravated. In the wiring structure where all conventional wiring intersects perpendicularly especially, it is between wiring which adjoins within the same layer and runs in parallel, and when doing effect mutually, even if it replaces wiring with other wiring layers, it will run in parallel by the upper and lower sides too. For this reason, it is difficult to mitigate the coupling capacity during wiring which runs in parallel within this layer.
[0008] In addition to the wiring structure which intersects perpendicularly, in relation to rectangular mold multilayer-interconnection structure, the wiring technique which shortens a wire length using wiring of the direction of slant (45 degrees or 135 degrees) is proposed. For example, the wiring technique of this direction of slant is indicated by automatic-layout approach" of a JP,5-102305,A" semiconductor integrated circuit. This conventional technique is explained.
[0009] Drawing 28 is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit equipment of the conventional technique using wiring of this direction of slant.
[0010] This wiring structure forms the wiring grid of the direction of slant as another layer on the layer which constitutes rectangular coordinates. 401 in drawing 28 is the wiring grid (grid) of the 1st layer, it

intersects perpendicularly with the upper layer, and the wiring grid 402 of the 2nd layer is formed. Furthermore, the 1st layer of the 1st layer of the 4th-layer wiring grid 404 of the direction of 135-degree slant is formed in these upper layers to 401 to 401 with the 3rd-layer wiring grid 403 of the direction of 45-degree slant.

[0011] However, the multilayer-interconnection technique of this conventional technique in which wiring of the direction of slant was used had the following troubles.

[0012] (1) With the conventional multilayer-interconnection structure, since the wiring grid of the direction of slant was prepared simply, there was a problem that the lattice point shifted. That is, as shown in drawing 29 , the 1st layer of the 2nd layer of the lattice point of 402 is set to 501 to 401. On the other hand, the 3rd layer of the 4th layer of the lattice point of 404 is set to 502 to 403. Here, when putting the 4th layer (beer hall) of the 3rd layer of a connection hole on 403 from 404, it will place at the lattice point 502. On the other hand, when putting the 3rd layer of the 2nd layer of a beer hall on 402 from 403, it will place at the lattice point 501. However, a beer hall cannot be placed if these lattice points 502 and 501 are approaching. For this reason, it will be necessary to establish a beer hall in another location. Thus, the wiring design was complicated when the lattice point shifted among the hierarchies of the upper slanting wiring grid (it is [403 and] 404 the 4th layer the 3rd layer) and a lower layer X-Y wiring grid (it is [401 and] 402 the 2nd layer the 1st layer).

[0013] (2) Resistance of the upper slanting wiring layer becomes being the same as that of a lower layer wiring layer. For this reason, even if it uses a slanting wiring layer for the upper layer, RC delay resulting from wiring is not reduced. Here, RC delay is delay by the resistance component R and the capacity component C. For this reason, even if it uses the upper slanting wiring grid, wiring structure suitable for global wiring for connecting a long distance cannot be built.

[0014] (3) Generally about the wiring pitch of the upper slanting wiring layer, it does not have a large pitch from the minimum design rule. For this reason, it does not have composition which mitigates the wiring capacity which adjoins even if it arranges a slanting wiring layer in the upper layer. The 2nd technique in which a limit of arrangement wiring spacing by the design rule arranges wiring of the severest layer aslant to the wiring grid on CAD is indicated by JP,7-86414,A" semiconductor device" about this point. However, since this conventional technique is not the configuration of taking large wiring width of face to coincidence, it cannot mitigate the above-mentioned wiring resistance. Moreover, since coupling capacity with contiguity wiring is not mitigated, RC delay of wiring is unmitigable.

[0015] (4) The configuration of a beer hall was defined as the rectangle configuration with the conventional technique. However, when connecting wiring other than wiring which intersect perpendicularly (i.e., when connecting wiring which crosses aslant), required sufficient cut area cannot be secured in a rectangular beer hall configuration. Therefore, the resistance over the electromigration phenomenon which causes a poor open circuit of wiring was inadequate.

[0016] (5) The relation of the definition of a cel low and the definition of a slanting wiring grid which arrange a logic cell to seriate and are formed was not clear. for this reason -- for example, when a total of four wiring layers of the two wiring layers and two slanting wiring layers which intersect perpendicularly were defined, it was clear that the wiring resources located in a cel low and parallel run short. Two wiring layers of the direction of slant are defined about this point on three wiring layers which intersect perpendicularly, and the technique which solves the problem that the above-mentioned wiring resource is insufficient is indicated by JP,5-243379,A" semiconductor integrated circuit equipment." However, with this technique, the wiring layer of five layers is needed and there is a problem of causing the rise of cost.

[0017] (6) The cross talk noise which causes malfunction of a circuit was not able to be reduced within the same wiring layer. In the wiring structure equipped with the slanting wiring grid of the conventional technique, an up-and-down wiring layer does not lap in the same wiring direction. For this reason, since the coupling capacity during wiring of an up-and-down wiring layer becomes small, the problem of the cross talk noise during vertical wiring is solved. However, within the same wiring layer, since different wiring is arranged in parallel, the coupling capacity during contiguity wiring is unmitigable. That is,

with the conventional slanting wiring grid technique, the cross talk noise which is between two wiring which is parallel within the same wiring layer, and is produced was unremovable.

[0018] (7) The conventional slanting wiring grid was inadequate for considering as wiring for current supply. For example, when it constitutes a pad in the core region of the chip which constitutes a combinational circuit, it is possible to use a part of this pad for current supply. (In addition, the boundary region which arranges I/O of a chip is called an I/O field to this core region.) The upper slanting wiring latticed layer can be used as auxiliary wiring for current supply in this case. In such a configuration, the conventional slanting wiring grids structure has become with structure with a wiring pitch unsuitable for constituting broad wiring, or wiring width of face. For this reason, it was the structure of not being suitable for using the upper slanting wiring latticed layer effectively as an object for current supply.

[0019] (8) Since the wire length of wiring which supplies a clock to the flip-flop in a chip from PLL (Phase Locked Loop) was long, delay was increasing.

[0020] In order that PLL may not worsen the property of the analog circuit built in a chip, it is usually arranged at the corner of a chip and is wired from this corner to each flip-flop. For this reason, wiring of die length also with the shortest near the semicircle enclosure length of a chip needed to be drawn. Therefore, while delay increased, when the number of stages of a buffer increased, the bad influence was in the duty ratio of a clock.

[0021] (9) In the case of memory circuits, such as SRAM, wiring which passes through these memory circuit top starts the coupling noise between wiring in memory, and passage wiring, and worsens the engine performance. For this reason, passage wiring on this memory circuit was avoided conventionally, and the wiring design was made. There is a conventional technique which shields passage wiring on this memory circuit. However, with this technique, in order to shield wiring, one more layer is needed further. Therefore, the configuration of a circuit was complicated. Moreover, there are other conventional techniques which use passage wiring on a memory circuit for small-size width-of-face signals. However, with this technique, the integrated circuit used as the candidate for application was limited.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, while the delay characteristics and noise resistance of a circuit improve, according to this invention, in addition to the wiring grid which intersects perpendicularly in the direction of X-Y, easy-izing of a wiring design and reduction-ization of a manufacturing cost are realized by utilizing a slanting wiring layer in the semiconductor integrated circuit using the multilayer-interconnection structure which prepared the wiring grid which intersects perpendicularly in the direction of slant.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] This invention is made in order to solve the above-mentioned trouble of the conventional technique.
[0023] and the wiring grid to which the purpose intersects perpendicularly in the direction of X-Y -- in addition, in the semiconductor integrated circuit using the multilayer-interconnection structure which prepared the wiring grid which intersects perpendicularly in the direction of slant, by utilizing a slanting wiring layer, while raising the delay characteristics and noise resistance of a circuit, it is in offering the semiconductor integrated circuit and the semiconductor integrated circuit wiring approach which enabled easy-izing of a wiring design, and reduction-ization of a manufacturing cost.

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MEANS

[Means for Solving the Problem] With wiring of m (m>=2) layer with which the description of this invention is formed in the upper layer of the semiconductor region in which two or more unit element children were formed, and said semiconductor region, and the n-th-1st-layer wiring and the n-th (n>=2) layer wiring cross at right angles mutually With the m+1st-layer wiring and the m+2nd-layer wiring which are located in the criteria wiring layer which forms the criteria wiring grid of the direction of X-Y, and the upper layer of said criteria wiring layer, and intersect perpendicularly mutually The slanting wiring layer which forms the slanting wiring grid which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring grid is provided. Said slanting wiring layer While being set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring The wiring width of face of the m+1st-layer wiring and said m+2nd-layer wiring is in the point of offering the semiconductor integrated circuit equipment characterized by being set up root2 twice to the wiring width of face of each layer of said criteria wiring layer.
[0025] Moreover, as for said slanting wiring layer, the wiring thickness has other descriptions of this invention in the point set up root2 twice of the wiring thickness of said criteria wiring grid.
[0026] Moreover, as for said criteria wiring layer and said slanting wiring layer, other descriptions of this invention constitute a wiring channel field, and said wiring channel field is in the point established in the direction parallel to the cel low which has arranged to seriate the logic cell which consists of said unit element child.
[0027] Moreover, in other descriptions of this invention, wiring of said criteria wiring layer and wiring of said slanting wiring layer establish the beer hall for wiring connection in these crossover parts, and said beer hall is in the point that the cross section is the configuration of either a hexagon, an octagon and a parallelogram.
[0028] Moreover, as for said two or more unit element children, other descriptions of this invention constitute a cel, and said cel is in the point of having the obstruction field which is defined by the configuration where it met in the wiring direction of said slanting wiring grid and where wiring is not performed.
[0029] Moreover, wiring of said slanting wiring layer has other descriptions of this invention in the point that the part is constituted as power-source wiring for current supply.
[0030] Other descriptions of this invention moreover, said two or more unit element children The cel which consists of said two or more unit element children is constituted. Said cel A clock signal is supplied by the wiring path of a tree mold. Said tree type of wiring path The 1st connection by the path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 1st and 2nd points, It is in the point constituted combining the unit wiring configuration constituted by connecting the 2nd connection by the path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 3rd and 4th points with wiring of said criteria wiring layer.
[0031] Other descriptions of this invention moreover, the above-mentioned semiconductor integrated circuit equipment the [furthermore, / which is located in the upper layer of said slanting wiring layer,

and intersects perpendicularly mutually] -- with p-1 (p>=2) layer wiring and the p-th-layer wiring The up wiring layer which forms the up wiring grid which crosses at the include angle of 45 degrees or 135 degrees to said slanting wiring grid or the p-th-2nd-layer wiring is provided. Said up wiring layer While being set up root2 twice to the wiring pitch of said the p-th-2nd-layer wiring between wiring of each layer of said slanting wiring layer, the wiring pitch during wiring of each class The wiring width of face of wiring of each class is in the point set up root2 twice to the wiring width of face of wiring of each layer of said slanting wiring layer, or said the p-th-2nd-layer wiring.

[0032] Moreover, said slanting wiring layer has other descriptions of this invention in the point that global wiring covering the whole chip is wired in general.

[0033] Moreover, said criteria wiring layer has other descriptions of this invention in the point that local wiring other than said global wiring is wired.

[0034] Moreover, as for said two or more unit element children, other descriptions of this invention constitute a cel, and when direct continuation of said cel should be carried out to said global wiring, it is in the point of having the output terminal configuration in which wiring and direct continuation of said slanting wiring layer are possible.

[0035] Other descriptions of this invention moreover, the above-mentioned semiconductor integrated circuit equipment A flip-flop circuit and PLL (Phase Locked Loop) arranged at the corner of a chip are provided. Furthermore, said flip-flop circuit A clock signal is supplied by the wiring path of a tree mold. Said tree type of wiring path It is in the point by which connection is carried out near the chip center using wiring of said slanting wiring layer from said PLL, and connection is carried out hierarchical so that RC product may be made to balance through a buffer cel to said flip-flop circuit near [said] the chip center.

[0036] Moreover, other descriptions of this invention possess the SRAM circuit where the above-mentioned semiconductor integrated circuit equipment uses wiring of said criteria wiring layer for wiring of the interior further, and said slanting wiring layer is in the point that wiring which passes through said SRAM circuit top is wired.

[0037] Moreover, said criteria wiring layer is constituted for other descriptions of this invention by three layers, and the point wired in the direction parallel to the cel low which has arranged to seriate the logic cell which consists of said unit element child has the 1st-layer wiring and the 3rd-layer wiring of said criteria wiring layer.

[0038] Moreover, said criteria wiring layer has other descriptions of this invention in the point constituted by two-layer.

[0039] With moreover, wiring of m (m>=2) layer which is the semiconductor integrated circuit wiring approach that other descriptions of this invention wire the component of a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring grid While being set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring The wiring width of face of the m+1st-layer wiring and said m+2nd-layer wiring is in the point of offering the semiconductor integrated circuit wiring approach characterized by including the step formed in order to be set up root2 twice to the wiring width of face of each layer of said criteria wiring layer.

[0040] Moreover, other descriptions of this invention are in the above-mentioned semiconductor integrated circuit wiring approach to the point containing the step which inserts the buffer cel for signal magnification in the step which extracts the wiring network which produces the delay which exceeds a predetermined time delay further out of the wiring network which said criteria wiring layer constitutes, and a location connectable with wiring of said slanting wiring layer on said extracted wiring network.

[0041] Moreover, the above-mentioned semiconductor integrated circuit wiring approach has other descriptions of this invention in the point containing the step which defines further the cel which consists of said two or more unit element children, and the step which defines the obstruction field

where wiring is not performed in said cel by the configuration where it met in the wiring direction of said slanting wiring layer.
[0042] Moreover, said obstruction domain-defined step has other descriptions of this invention in the point which arranges said m+1st-layer wiring or said m+2nd-layer wiring near [the] the corner.
[0043] Moreover, further, the above-mentioned semiconductor integrated circuit wiring approach is wiring of said either of m layers of said criteria wiring layer, and other descriptions of this invention are in the point containing the step which replaces the predetermined part in the middle of one wiring of said wiring of two with wiring of said slanting wiring layer, when one wiring exerts a noise on wiring of another side among parallel wiring of two belonging to the same layer.
[0044] Moreover, the above-mentioned semiconductor integrated circuit wiring approach has other descriptions of this invention in the point containing the step which inserts a buffer cel further into the path of wiring of said slanting wiring layer used for said replacement.
[0045] With moreover, wiring of m (m>=2) layer which is the cel configuration method which, as for other descriptions of this invention, arranges a cel on a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The cel which consists of two or more unit element children It is in the point of offering the cel configuration method characterized by including the step arranged based on the predetermined cutting method using the cutline of the direction of X-Y corresponding to the wiring direction of said criteria wiring layer, and the cutline of the direction of slant corresponding to the wiring direction of said slanting wiring layer.
[0046] Other descriptions of this invention moreover, the above-mentioned semiconductor integrated circuit wiring approach Furthermore, the step which sets up the 1st path formed so that it might approach each other in the wiring top of said slanting wiring layer from the 1st and 2nd points, The step which sets up the 2nd path formed so that it might approach each other in the wiring top of said slanting wiring grid from the 3rd and 4th points, The step which forms the unit wiring configuration constituted by connecting said the 1st path and said 2nd path with wiring of said criteria wiring layer, It is in the point which contains the step which forms the wiring path of the tree mold which supplies a clock signal in the cel which consists of said two or more unit element children combining said unit wiring configuration.
[0047] With moreover, wiring of m (m>=2) layer which is the semiconductor integrated circuit wiring approach that other descriptions of this invention wire the component of a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, The step connected near the chip center using wiring of said slanting wiring layer from PLL (Phase Locked Loop) arranged at the corner of a chip, It is in the point of offering the semiconductor integrated circuit wiring approach characterized by including the step connected hierarchical so that RC product may be made balancing through a buffer cel to said flip-flop circuit in said chip near [said] the chip center.
[0048] With moreover, wiring of m (m>=2) layer which is the semiconductor integrated circuit wiring approach that other descriptions of this invention wire the component of a semiconductor integrated circuit, and intersects perpendicularly as mutually [the n-th (n>=2) layer wiring] as the n-th-1st-layer wiring With the m+1st-layer wiring and the m+2nd-layer wiring which intersect perpendicularly with the step which forms the criteria wiring layer of the direction of X-Y mutually The slanting wiring layer

which crosses at the include angle of 45 degrees or 135 degrees to said criteria wiring layer The step which the wiring pitch during the m+1st-layer wiring and during the m+2nd-layer wiring forms so that it may be set up root2 twice to the wiring pitch during wiring of each layer of said criteria wiring layer, It is in the point of offering the semiconductor integrated circuit wiring approach characterized by including the step which forms the SRAM circuit which uses wiring of said criteria wiring layer for wiring of the interior, and the step which forms wiring which passes through said SRAM circuit on said slanting wiring layer.

[0049]

[Embodiment of the Invention] Hereafter, with reference to a drawing, the operation gestalt of the semiconductor integrated circuit concerning this invention and the semiconductor integrated circuit wiring approach is explained to a detail.

[0050] The operation gestalt of the 1st operation gestalt 1st in the upper layer of the criteria wiring grid of the 1st layer which intersects perpendicularly mutually, and the 2nd layer Cross at the include angle of 45 degrees or 135 degrees to this criteria wiring grid, and the slanting wiring grid formed with the 3rd-layer wiring which intersects perpendicularly mutually, and the 4th-layer wiring is prepared. While shortening a wire length by having set up the wiring pitch and wiring width of face during the 3rd-layer wiring of this slanting wiring grid, and during the 4th-layer wiring root2 twice to the wiring pitch of a criteria wiring grid, it is the operation gestalt which reduced RC delay and raised noise resistance.

[0051] Drawing 1 is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit equipment concerning the 1st operation gestalt of this invention. Drawing 2 is the top view showing an example of the wiring structure at the time of wiring based on wiring grids structure as shown in drawing 1 . Moreover, drawing 3 is the A-A sectional view of drawing 4 .

[0052] As shown in drawing 1 , as for the wiring structure of the 1st operation gestalt, the 3rd layer and 4th-layer wiring equips the wiring list of the 1st layer and the 2nd layer with the wiring grid which intersects perpendicularly mutually like the conventional technique of drawing 28 . That is, to the 1st layer, the grid is arranged so that the 3rd layer and the 4th layer may cross at 45 degrees and 135 degrees, respectively.

[0053] One in drawing 1 is the wiring grid of the 1st layer, it intersects perpendicularly with the upper layer, and the wiring grid 2 of the 2nd layer is formed. Furthermore, sequential arrangement of the 4th-layer wiring grid 4 of the direction of 135-degree slant is carried out to the 3rd-layer wiring grid 3 and the 1st-layer wiring grid 1 of the direction of 45-degree slant to the 1st-layer wiring grid 1.

[0054] Here, the 1st operation gestalt sets up more widely than between the 1st-layer wiring 1 and between the 2nd-layer wiring 2 the wiring pitch between the 4th-layer wiring 4 between the 3rd-layer wiring 3 arranged in the direction of slant, respectively. Specifically, the wiring pitch between the 3rd-layer wiring 3 and between the 4th-layer wiring 4 is set up root2 twice (root2andlambda) of the wiring pitch (lambda) between the 1st-layer wiring 1 and between the 2nd-layer wiring 2.

[0055] Thereby, it is avoidable that the lattice point shifts among the hierarchies of the upper X-Y wiring grid (it is [4 and] 4 the 4th layer the 3rd layer) and a lower layer slanting wiring grid (it is [1 and] 2 the 2nd layer the 1st layer). For this reason, it becomes possible to easy-ize a wiring design. That is, the beer hall between the 2nd layer and the 3rd layer can be established in the intersection of the grid of the 1st layer and the 2nd layer, and the adjoining grid can be used for the 1st layer or 2nd-layer wiring.

[0056] Furthermore, the 1st operation gestalt sets up more widely than the 1st-layer wiring 1 and the 2nd-layer wiring 2 the wiring width of face of the 3rd-layer wiring 3 and the 4th-layer wiring 4 arranged in the direction of slant in the wiring pitch (root2andlambda). As shown in drawing 2 , specifically, the wiring width of face of the 3rd-layer wiring 3 and the 4th-layer wiring 4 is set up root2 twice (root2andd) of the wiring width of face (d) of the 1st-layer wiring 1 and the 2nd-layer wiring 2, respectively. As mentioned above, since the wiring pitch of the 3rd layer and the 4th layer has root2 doubled, wiring spacing which p of drawing 2 shows does not have breaking a design rule. For this reason, wiring width of face can be expanded, without conflicting with a design rule.

[0057] In the example shown in drawing 3 , the 1st-layer wiring 1 is arranged perpendicularly first, and

the 2nd-layer wiring 2 is arranged in the direction which intersects perpendicularly with it. On the other hand, the 3rd-layer wiring 3 and the 4th-layer wiring 4 are arranged in the direction of slant. 12 in drawing is the beer hall placed between the 1st-layer wiring 1 and the 2nd-layer wiring 2, 13 is the beer hall placed between the 2nd-layer wiring 2 and the 3rd-layer wiring 3, and further 14 is the beer hall placed between the 3rd-layer wiring 3 and the 4th-layer wiring 4.

[0058] The 1st operation gestalt has set up more thickly than the 1st-layer wiring 1 and the 2nd-layer wiring 2 the wiring thickness of the 3rd-layer wiring 3 and the 4th-layer wiring 4 arranged in the direction of slant on the assumption that the description of the above-mentioned wiring pitch and wiring width of face. As shown in drawing 3 , specifically, the wiring thickness of the 3rd-layer wiring 3 and the 4th-layer wiring 4 is set up root2 twice (root2andt) of the wiring width of face (t) of the 1st-layer wiring 1 and the 2nd-layer wiring 2, respectively. In addition, ten in drawing 3 is a semi-conductor substrate with which a transistor is formed, and 11 is an interlayer insulation film. By using the structure which made the above-mentioned wiring width of face of the 3rd layer and the 4th layer and wiring thickness the 1st layer and twice [root2] the 2nd layer, the wiring cross section of the 3rd-layer wiring and the 4th-layer wiring becomes twice the wiring cross section of the 1st-layer wiring and the 2nd-layer wiring, as shown in the following formulas.

[0059] root2xroot2=2, for this reason the wiring resistance per unit length are set to one half of the 1st layer and 2nd-layer wiring. On the other hand, although the opposed face product with contiguity wiring becomes root2 twice, since contiguity wiring spacing also becomes root2 twice, it is the same as that of the capacity between contiguity wiring in the 1st-layer wiring and the 1st-layer wiring. [of the capacity between contiguity wiring in the 3rd-layer wiring and the 4th-layer wiring] Since the capacity between contiguity wiring has the same wiring resistance at one half, the wiring RC delay per unit length is set to one half of the 1st layer and 2nd-layer wiring. In addition, delay according [wiring RC delay] to the resistance component and capacity component of wiring is said.

[0060] As mentioned above, according to the 1st operation gestalt, the wiring pitch during the 3rd-layer wiring and during the 4th-layer wiring is set up root2 twice to the wiring pitch during the 1st-layer wiring and during the 2nd-layer wiring. For this reason, it can avoid that the lattice point shifts among the hierarchies of the upper slanting wiring grid and a lower layer criteria wiring grid, and it becomes possible to easy-ize a wiring design.

[0061] Moreover, since wiring width of face was also set up root2 twice, wiring RC delay can be reduced. Furthermore, since wiring thickness was also set up root2 twice, wiring RC delay can be reduced further and big effectiveness is acquired from a viewpoint of raising a speed of a circuit of operation by comparatively long wiring.

[0062] The operation gestalt of the 2nd operation gestalt 2nd is an operation gestalt which inserts a repeater cel (buffer cel) in wiring, and prevents generating of the timing error by wiring delay further in the multilayer-interconnection structure using the slanting wiring grid of the 1st operation gestalt.

[0063] Drawing 4 (a), (b), (c), and (d) are drawings showing the insertion procedure of the repeater cel of the 2nd operation gestalt. Drawing 5 (a) and (b) are drawings for explaining wiring delay. With reference to drawing 4 and drawing 5 , the insertion procedure of the repeater cel of the 2nd operation gestalt is explained concretely.

[0064] First, all networks are wired with wiring of only the direction of X-Y only using the 1st layer and the 2nd layer. Next, delay analysis is performed using a simulator and the network which has started the timing error is extracted. The following processings are performed to this extracted network.

[0065] That is, a repeater cel is inserted to the network which started the timing error. As an insertion location of this repeater cel, the 3rd layer and the 4th layer are used and a repeater cel is inserted in a location connectable with wiring of the direction of slant. A wire length can be shortened by using the 3rd layer or the 4th layer.

[0066] For example, the timing error should occur in a network as shown in drawing 4 (d). In this network, three kinds, drawing 4 (a), (b), and (c), can be considered as the insertion point of the repeater cel 20 between a cel 21 and a cel 22, and a direction of wiring. In the example of drawing 4 (a), after using the wiring 23 of the direction of X first and then inserting the repeater cel 20, the slanting wiring

25 is used. In the example of drawing 4 (b), after inserting the repeater cel 20 first and using the wiring 34 of the direction of slant, the wiring 35 of the direction of X is used. In the example of drawing 4 (c), after inserting the repeater cel 20 first and using the wiring 45 of the direction of X, the wiring 46 of the direction of slant is used.

[0067] A difference of the insertion point of the repeater cel of drawing 4 (a), (b), and (c) produces the difference of allocation of delay with between the repeater cel 20 and the cel 22 which carries out a signal input between the cel 21 which outputs a signal, and the repeater cel 20. When the example of drawing 4 (a) and drawing 4 (b) is compared, the delay between a cel 21 and the repeater cel 20 has less drawing 4 (b) than the example of drawing 4 (a). On the other hand, the delay between the repeater cel 20 and a cel 22 has less drawing 4 (a) than the example of drawing 4 (b). It is dependent on the transistor size of a cel 21 and the repeater cel 20 which example can make actual delay small. Therefore, it is necessary to analyze delay in all the combination that can be considered generally, and to determine the operation of the insertion point of a final repeater, and the wiring direction. However, in the example of drawing 4 (c), delay becomes large compared with other examples clearly.

[0068] About wiring width of face, if the wiring delay formula of ERUMOA is followed, as for wiring delay, the direction gradually made thin from the cel which carries out the signal output of the wiring width of face will become short. That is, wiring delay becomes [using the thick wiring width of face 74 rather than / as those who continued using the first thick wiring width of face 63 as shown in drawing 5 (a), and used the thin wiring width of face 64 show drawing 5 (b), continue using the first thin wiring 73, and] short.

[0069] wiring with which wiring of the direction of slant met X and a Y-axis -- root -- since it is thick twice, wiring delay becomes short rather than the case where the direction at the time of having used wiring of the direction of slant first, and using wiring of X or the direction of Y continuously continues first using wiring of X or the direction of Y, and uses wiring of the direction of slant. That is, it is understood from the example of drawing 4 (c) that, as for wiring delay, the direction of the example of drawing 4 (b) becomes short.

[0070] Therefore, the Ruhr at the time of inserting a repeater cel by the case where slanting wiring is used is specified as follows.

[0071] (1) Connect slanting wiring to wiring near the output terminal of a signal.
(2) Connect slanting wiring to the output terminal of a signal.
(3) Use slanting wiring abundantly to wiring near the signal output terminal of a repeater cel.
(4) Connect wiring of the direction of slant to the signal output terminal of a repeater cel.
(5) Arrange a repeater cel in the location which can connect slanting wiring to a signal output terminal.

[0072] If the above Ruhr is followed, the structure of a repeater cel will also be specified as follows.

[0073] (1) Form a signal input terminal so that it may become easy to connect with wiring which met in the direction of X-Y. That is, a signal input terminal is made to the 1st layer.
(2) Further, a signal output terminal is formed so that connecting with wiring of the direction of slant may become easy. That is, a signal output terminal is made to the 3rd layer.

[0074] As mentioned above, in order to prevent generating of the timing error by wiring delay, in case the repeater cel which relays and amplifies a signal is inserted on a wiring network according to the 2nd operation gestalt, a repeater cel is inserted in a location connectable with this slanting wiring grid using a slanting wiring grid. For this reason, a repeater cel can be inserted on the optimal conditions, a wire length can be shortened, and wiring delay can be reduced further.

[0075] The operation gestalt of the 3rd operation gestalt 3rd is an operation gestalt which prepares a wiring channel in the direction parallel to a cel low, and cancels the lack of a wiring resource of the direction of a cel low in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.

[0076] Drawing 6 is the layout pattern showing the configuration of the semiconductor integrated circuit concerning the 3rd operation gestalt of this invention.

[0077] two or more cel lows which the semiconductor integrated circuit of drawing 6 arranged the logic cell to seriate, and were formed -- it has 80. two or more of these cel lows -- the multilayer

interconnection which has the slanting wiring grid shown in drawing 1 is formed in the upper part of 80.

[0078] Specifically one in drawing 6 is the 1st-layer metal wiring, 2 is the 2nd-layer metal wiring, and 3 is the 3rd-layer metal wiring, and 4 is the 4th-layer metal wiring. the configuration of drawing 6 -- setting -- each -- the wiring channel 85 which consists of each metal wiring 1, 2, 3, and 4, respectively is formed in the direction parallel to cel low 80. namely, a cel low -- the wiring channel 85 is formed in the direction parallel to 80. For this reason, the wiring resource of the direction of a cel low which requires more wiring resources is securable with few wiring hierarchies.
[0079] As mentioned above, according to the 3rd operation gestalt, by few wiring hierarchies, the lack of a wiring resource of the direction of a cel low which requires more wiring resources can be canceled, and a wiring resource can be secured.
[0080] In the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt, the operation gestalt of the 4th operation gestalt 4th is an operation gestalt which improved the configuration so that the cut area of the beer hall which connects wiring which crosses aslant may not become inadequate.
[0081] Drawing 7 (a), (b), (c), and (d) are the part plans showing the configuration of the beer hall of the semiconductor integrated circuit concerning the 4th operation gestalt, respectively.
[0082] In the multilayer-interconnection structure of having the slanting wiring grid which showed the semiconductor integrated circuit concerning the 4th operation gestalt to drawing 1 When the direction wiring of X-Y (the 1st layer or the 2nd layer) and the direction wiring of slant (the 3rd layer or the 4th layer) which accomplishes the include angle of 45 degrees or 135 degrees to this are connected As shown in drawing 7 (a), (b), (c), and (d), The longitudinal section uses the beer hall of an octagon, a parallelogram, or a hexagon. By using the beer hall of these cross-section configurations, the beer hall cut of sufficient cross-sectional area required between the crossing wiring layers can be created.
[0083] Beer hall 90A of an octagon is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (a). Moreover, beer hall 90B of a parallelogram is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (b).
[0084] In addition, it is possible that beer halls approach unusually with the example shown in drawing 7 (b). In order to avoid this, the configuration of the hexagon shown in drawing 7 (c) and drawing 7 (d) is offered. Beer hall 90C of a hexagon is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (c). Moreover, beer hall 90D of a hexagon is formed in the crossing of the direction wiring 91 of X-Y, and the direction wiring 92 of slant in the example of drawing 7 (d).
[0085] As mentioned above, according to the 4th operation gestalt, let the cross-section configuration of a beer hall of connecting wiring which crosses aslant be an octagon, a parallelogram, or a hexagon. For this reason, the cut area of the beer hall which connects wiring which crosses aslant is fully secured. The operation gestalt of the 5th operation gestalt 5th is an operation gestalt which defines the obstruction field of wiring the optimal in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0086] Drawing 8 (a) and (b) are drawings showing the cel or mega cell in the semiconductor integrated circuit concerning the 5th operation gestalt of this invention.
[0087] 101 shown in drawing 8 (a) is the cel in which two or more unit element children were formed, or the mega cell which carried out two or more sets of these cels. This cel or mega cell 101 is divided into the service area 102 and the transistor field 103 bordering on 45-degree Rhine 101a of those four corners. In the transistor field 103, a transistor and low order hierarchy cel 103a are arranged. On the other hand, it is prepared in a service area 102 in order to use effectively the four corners of a cel (are mentioned later) for the purpose of easing the wiring confusion produced near [four-corners] a cel, and neither a transistor nor a low order hierarchy cel is arranged. In addition, a cel is explained as a thing containing the above-mentioned mega cell below.
[0088] furthermore, as shown in drawing 8 (b), especially wiring arranged to the transistor field 103 of

the above-mentioned cel 101 was mentioned above near the four-corners Rhine 101a -- it is good to use 45 degrees of 135-degree slanting wiring 113 again.
[0089] Thus, in case a cel or a mega cell is designed, the form where slanting wiring (45 degrees or 135 degrees) was met can define the obstruction of wiring by preparing the above-mentioned service area and making it the configuration which does not use the four corners. Next, this point is explained.
[0090] Drawing 9 (a) and (b) are drawings showing the example of the obstruction of wiring concerning the 5th operation gestalt. In the example shown in drawing 9 (a), the obstruction field in a cel 101 is made the definition by the set of the small rectangle 122. Here, an obstruction field is a field for defining the obstruction of wiring in a wiring design.
[0091] The example shown in drawing 9 (b) defines the obstruction field in a cel 101 by the polygon or its set. namely, the case where there are two obstruction fields in the example of drawing 9 (b) -- them -- a trapezoid -- it defines as 132,133, respectively.
[0092] Although there is a difficulty that the amount of data in a CAD design increases, in the example shown in drawing 9 (a), the example shown in drawing 9 (b) to this can define an obstruction field by the small amount of data.
[0093] Drawing 10 (a) and (b) are drawings showing the effectiveness of the 5th operation gestalt.
[0094] In the usual X-Y wiring grid model, as shown in drawing 10 (a), the obstruction field 142 of the cel or mega cell 141 interior is defined as a set of a rectangular rectangle. When rectangular wiring was performed using these cels or mega cells 141, there was a problem that the degree of integration of a chip fell owing to the increase of the congestion factor of the wiring 143 in the four-corners neighborhood 144 and it.
[0095] On the other hand, if it wires using the cel and mega cell 101 which were created by the technique of the 5th operation gestalt mentioned above, as shown in drawing 10 (b), the obstruction field 152 is defined by the configuration which does not use the four corners of a cel or a mega cell. The configuration where slanting wiring was met can define this obstruction field 152. For this reason, the congestion factor of the wiring 153 in the above-mentioned four-corners neighborhood 154 is eased, and the degree of integration of a chip improves.
[0096] As mentioned above, according to the 5th operation gestalt, an obstruction field is defined in the design of a cel or a mega cell by the configuration where slanting wiring was met with the configuration which does not use the four corners of a cel or a mega cell. For this reason, the four corners of a cel can be used effectively. Moreover, the congestion factor of wiring in the above-mentioned four-corners neighborhood is eased, and the degree of integration of a chip improves.
[0097] The operation gestalt of the 6th operation gestalt 6th is an operation gestalt which controls the cross talk noise produced when there is wiring arranged in parallel in this layer in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0098] Drawing 11 (a), (b), and (c) are drawings showing the important section of the configuration of the semiconductor integrated circuit concerning the 6th operation gestalt of this invention. In addition, the same sign is given to drawing 6 and a common element, and the explanation is omitted.
[0099] The case where there is wiring 161,162 arranged by being parallel in this layer as shown in drawing 11 (a) is considered. the 6th operation gestalt -- one of the wiring (for example, wiring 162) -- on the way -- a wiring layer is changed so that a part may be replaced with the direction wiring 173,174 of slant which accomplishes the include angle of this wiring 162, 45 degrees, or 135 degrees, as shown in drawing 11 (b). By replacement of this wiring, the distance to which two wiring of this layer becomes parallel becomes short, and can control generating of a cross talk noise.
[0100] Moreover, if the direction which receives a noise for the direction which generates a noise among the parallel wiring 161,162 with wiring 161 is assumed to be wiring 162, in case wiring 162 will be changed with the direction wiring 173,174 of slant mentioned above, one or more buffer cels 183 are inserted on the direction wiring 173,174 of slant.
[0101] Thus, it is possible by inserting a buffer cel into the path of the direction wiring of slant to prevent propagation of a noise completely. For example, if **** distance is restricted so that the voltage level of a cross talk noise produced between two wiring arranged in parallel in this layer may not exceed

the logic threshold of said buffer cel 183 inserted as an object for noise cancellation, it is possible to control a noise completely.
[0102] As mentioned above, according to the 6th operation gestalt, in the middle of wiring of one of wiring arranged by being parallel in this layer, a wiring layer is changed so that a part may be replaced with the direction wiring of slant. Moreover, a buffer cel is inserted into the path of the direction wiring of slant used for replacement. For this reason, the distance to which two wiring in the same layer becomes parallel becomes short, and generating of the cross talk noise during wiring is controlled.
[0103] The operation gestalt of the 7th operation gestalt 7th is an operation gestalt using the wiring resource of a slanting wiring grid as an object for current supply in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0104] Drawing 12 is drawing showing the important section configuration of the semiconductor integrated circuit concerning the 7th operation gestalt of this invention. The same sign is given to drawing 6 and a common element, and the explanation is omitted.
[0105] As shown in drawing 12 , some of 3rd-layer wiring 3 located in the upper layer of the 1st-layer wiring 1 and the 2nd-layer wiring 2 and 4th-layer wiring 4 are used for the wiring 191 for current supply for current supply. thereby -- the wiring resource of the common signal line of the direction of slant -- a part -- as the object for current supply -- using -- a cel low -- the power source which run short by 80 is suppliable.
[0106] As mentioned above, according to the 7th operation gestalt, a part of wiring resource of the general signal point of the direction of slant is used as wiring for current supply. For this reason, the power source which run short in a cel low is suppliable.
[0107] The operation gestalt of the 8th operation gestalt 8th is an operation gestalt which optimizes arrangement of a cel in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0108] Drawing 13 (a) and (b) are drawings showing the arrangement technique of the cel of the semiconductor integrated circuit concerning the 8th operation gestalt of this invention.
[0109] Usually, in the LSI design by CAD, the configuration method of a cel is performed in consideration of the ease of wiring so that a wire length may become short. The technique of the following which used the top-down technique is used for the activity of arranging which cel where, in that case.
[0110] By this conventional technique, as shown in drawing 13 (b), the set of the cel which it is going to arrange from now on is first divided into two by the cutline 260 in every direction. Next, a cel 201,210 is arranged so that the number of wiring which crosses this cutline 260 may decrease. This two piece housing is repeated until it halves after that still more nearly similarly using a cutline and all fields become the minimum unit. The above-mentioned conventional technique is called the mini cutting method.
[0111] Here, the conventional cutline 260 is the straight line of length and width corresponding to the wiring grid of the direction of X-Y, as shown in drawing 1313 (b). However, if the direction wiring of slant mentioned above is prepared, what has the include angle of 45 degrees as an obstruction of wiring as the 5th operation gestalt explained will appear. For this reason, the location of the optimal cel is no longer obtained only by the cutline 260 of length and width.
[0112] Then, as shown in drawing 13 (a), in addition to the cutline which intersects perpendicularly in all directions [conventional], the cutline 250 of the direction of slant is used for the 8th operation gestalt. A cel 201,210 is arranged so that the number of wiring which crosses the cutline 250 of this direction of slant may become min. The location of a cel can be decided to be able to perform optimal wiring in every direction and the direction of slant by this, and it becomes possible to raise the degree of integration of LSI.
[0113] As mentioned above, according to the 8th operation gestalt, in case arrangement of the cel in an LSI design is designed, cel arrangement is performed by the mini cutting method for using the cutline of the direction of slant. For this reason, the location of a cel can be optimized so that optimal wiring can be performed in the multilayer-interconnection structure using a slanting wiring grid. Therefore, the

degree of integration of LSI can be raised.
[0114] The operation gestalt of the 9th operation gestalt 9th is an operation gestalt which optimizes the configuration of the clock tree in the wiring design for the clock supply in the case of using the direction wiring of slant, and reduces dispersion in wiring RC delay in the multilayer-interconnection structure using the slanting wiring grid of the above-mentioned operation gestalt.
[0115] Drawing 14 (a), (b), (c), and (d) are drawings for explaining the basic configuration of the clock tree of the semiconductor integrated circuit equipment concerning the 9th operation gestalt of this invention.
[0116] In order to have the delay of a clock signal for every path pass, generally the wiring configuration of a tree mold is used. In this case, if only the direction of X-Y is the multilayer-interconnection structure of a wiring grid, as shown in general in drawing 14 (d), it will become the repeat of the wiring configuration of H mold shown in drawing 1414 (b).
[0117] In construction of such a tree wiring path, the 9th operation gestalt takes the repeat structure of the configuration where the direction wiring of slant as shown in drawing 14 (a) was utilized, as shown in drawing 14 (c). That is, as shown in drawing 14 (a), a path is connected so that it may approach each other using a slanting wiring grid from four points P1, P2, P3, and P4. in every direction at the points P5 and P6 where two points, P1, P2, and P3 and P4, were formed at a time -- the configuration of drawing 14 (a) is acquired by connecting with wiring of one of wiring layers. However, let the points P5 and P6 where a path branches be the locations to which the delay of the downstream of signal propagation is equal.
[0118] <A HREF="/Tokujitu/tjitemdrw.ipdl?N0000=239&N0500=1E_N/;>=?7=8;=?7=8;=?7=8;=?7=8;=?7=8;=?7=8;=?7=8;=?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8; =?7=8;

[Translation done.]

* NOTICES *

1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] It is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit equipment concerning the 1st operation gestalt of this invention.
[Drawing 2] It is the top view showing an example of the wiring structure at the time of wiring based on wiring grids structure as shown in drawing 1 .
[Drawing 3] It is the A-A sectional view of drawing 2 .
[Drawing 4] It is drawing explaining the repeater cel insertion technique of the semiconductor integrated circuit equipment concerning the 2nd operation gestalt of this invention.
[Drawing 5] It is drawing explaining wiring delay.
[Drawing 6] It is the layout pattern showing the configuration of the semiconductor integrated circuit equipment concerning the 3rd operation gestalt of this invention.
[Drawing 7] It is the part plan showing the configuration of the beer hall of the semiconductor integrated circuit equipment concerning the 4th operation gestalt of this invention.
[Drawing 8] It is drawing showing the cel or mega cell in the semiconductor integrated circuit equipment concerning the 5th operation gestalt of this invention.
[Drawing 9] It is drawing showing the example of the obstruction of wiring in the 5th operation gestalt.
[Drawing 10] It is drawing explaining the relation of the obstruction field of wiring and wiring in the 5th operation gestalt.
[Drawing 11] It is drawing showing the important section configuration of the semiconductor integrated circuit equipment concerning the 6th operation gestalt of this invention.
[Drawing 12] It is drawing showing the important section configuration of the semiconductor integrated circuit equipment concerning the 7th operation gestalt of this invention.
[Drawing 13] It is drawing showing the configuration method of the cel of the semiconductor integrated circuit concerning the 8th operation gestalt of this invention.
[Drawing 14] It is drawing explaining the basic configuration of the clock tree of the semiconductor integrated circuit concerning the 9th operation gestalt of this invention.
[Drawing 15] It is drawing explaining the modification of the configuration of the clock tree concerning the 9th operation gestalt.
[Drawing 16] It is drawing explaining the configuration of the tree important section at the time of establishing an alternate route.
[Drawing 17] It is drawing having shown the concrete wiring approach in case automatic wiring performs a slanting wiring grid.
[Drawing 18] It is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit concerning the 10th operation gestalt of this invention.
[Drawing 19] It is a sectional view at the time of observing the wiring grids structure of drawing 18 from X shaft orientations.
[Drawing 20] It is drawing explaining the wiring grids structure by global wiring and local wiring of a semiconductor integrated circuit concerning the 11th operation gestalt of this invention.

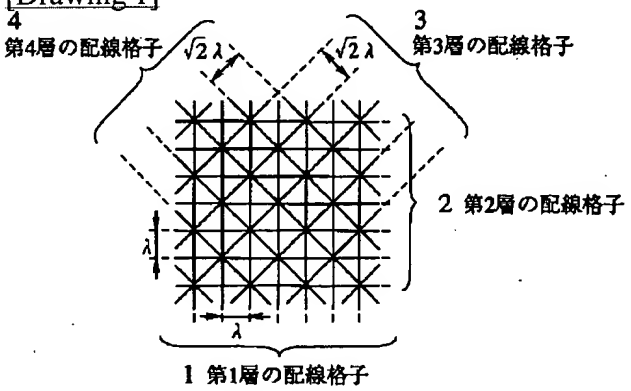
[Drawing 21] In the 11th operation gestalt, it is drawing explaining the direct continuation to wiring of a slanting wiring grid from a cel with the strong drive force.
[Drawing 22] It is drawing explaining the defining point of the output terminal of a cel with the strong drive force of drawing 21 .
[Drawing 23] It is drawing explaining the wiring structure of clock supply wiring to each flip-flop from PLL concerning the wiring structure of clock supply wiring to each flip-flop from the conventional PLL, and the 12th operation gestalt of this invention.
[Drawing 24] It is drawing explaining the wiring structure of clock supply wiring to each flip-flop from PLL concerning the 12th operation gestalt.
[Drawing 25] It is drawing explaining the clock tree structure of the 12th operation gestalt.
[Drawing 26] It is drawing explaining the clock tree structure of the 12th operation gestalt.
[Drawing 27] It is the layout pattern showing the wiring grids structure of the semiconductor integrated circuit concerning the 13th operation gestalt of this invention.
[Drawing 28] It is the layout pattern showing the wiring grids structure of the conventional semiconductor integrated circuit equipment using wiring of the direction of slant.
[Drawing 29] It is drawing explaining the trouble of a gap of the lattice point of the conventional technique.
[Description of Notations]
1,601 The 1st-layer wiring
2,602 The 2nd-layer wiring
3,603 The 3rd-layer wiring
4,604 The 4th-layer wiring
10 Semi-conductor Substrate
11 Interlayer Insulation Film
12, 13, 14 Beer hall
20 Repeater Cel
21 22,101,201 Cel
80 Cel Low
85 Wiring Channel
102 Service Area
103 Transistor Field
191 Wiring for Current Supply
250 260 Cutline
605 5th-Layer Wiring
610 Cel with Strong Drive Force
801 802 Clock wiring
803 PLL
804 Chip Pin Center,large
805 Buffer Cel
806 Flip-flop
807 Cluster
901 SRAM

[Translation done.]

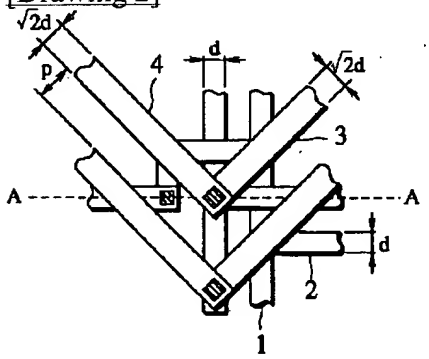
* NOTICES *

DRAWINGS

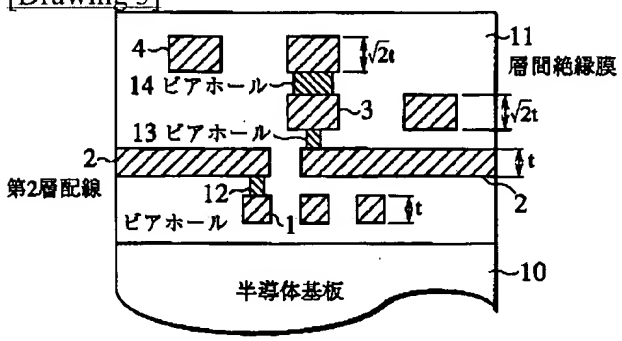
[Drawing 1]



[Drawing 2]

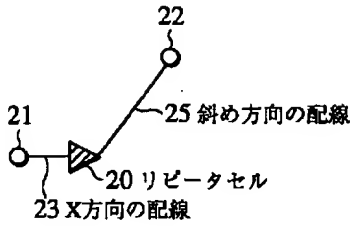


[Drawing 3]

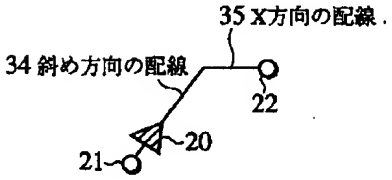


[Drawing 4]

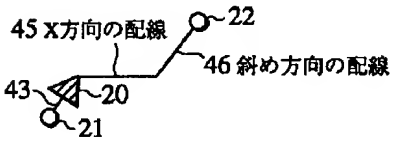
(a)



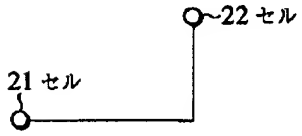
(b)



(c)

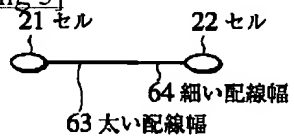


(d)

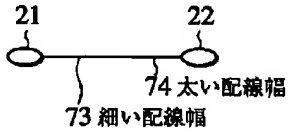


[Drawing 5]

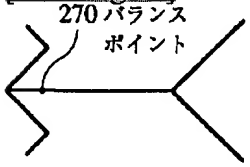
(a)



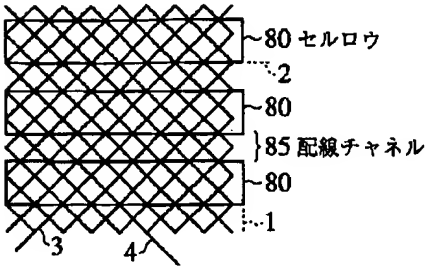
(b)



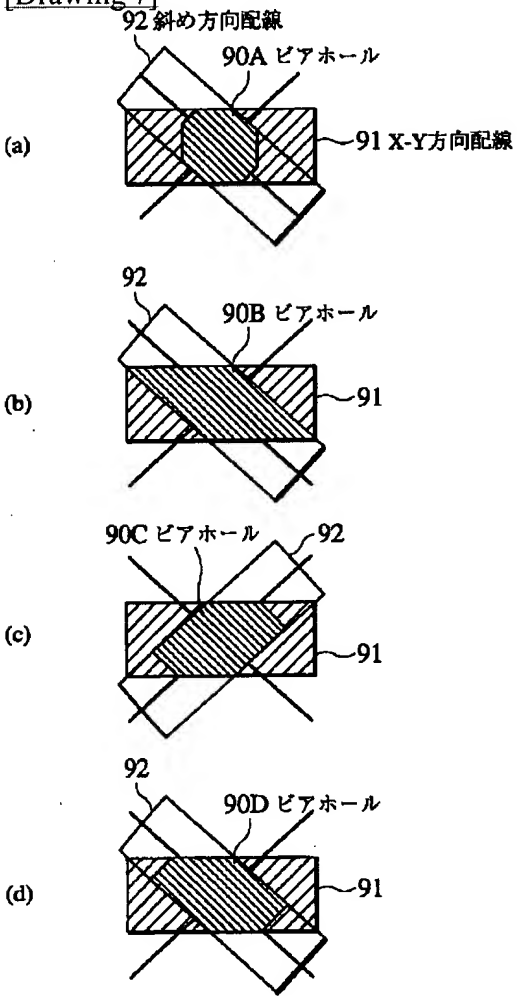
[Drawing 15]



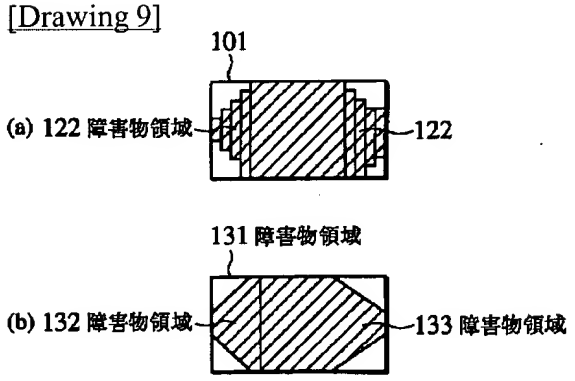
[Drawing 6]



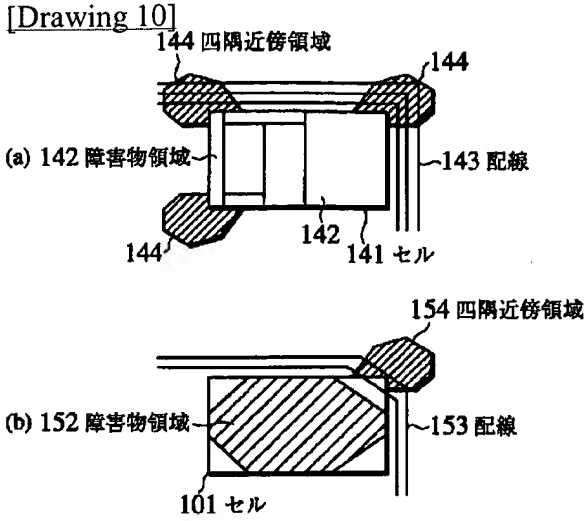
[Drawing 7]



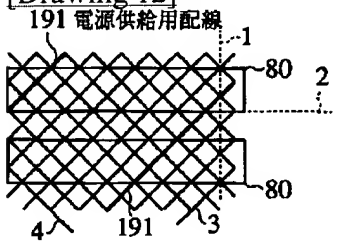
[Drawing 9]



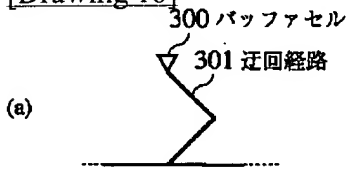
[Drawing 10]

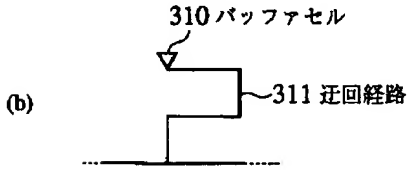


[Drawing 12]



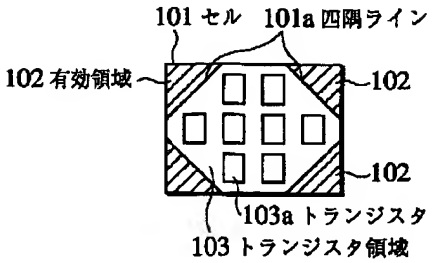
[Drawing 16]



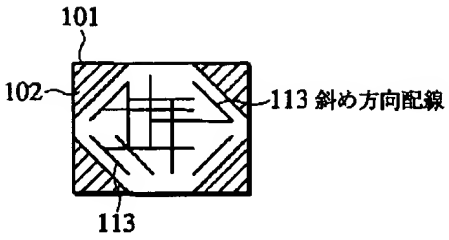


[Drawing 8]

(a)

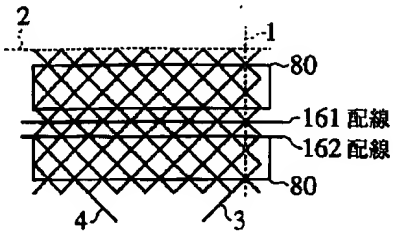


(b)

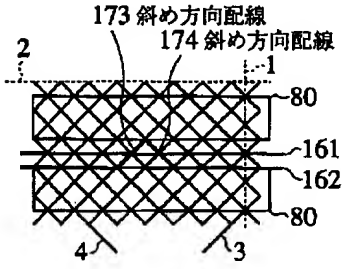


[Drawing 11]

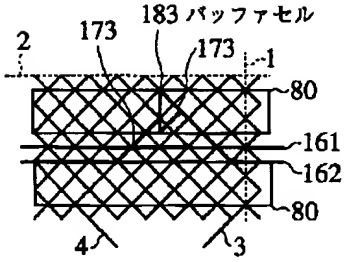
(a)



(b)

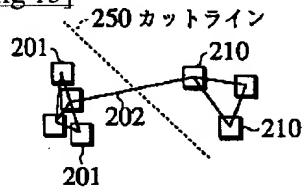


(c)

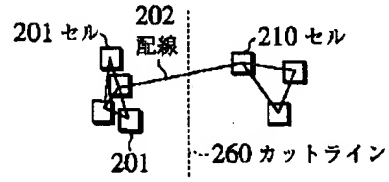


[Drawing 13]

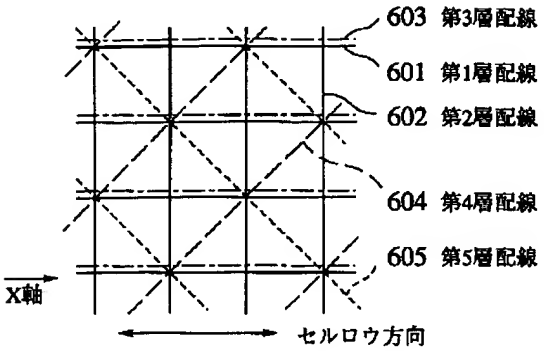
(a)



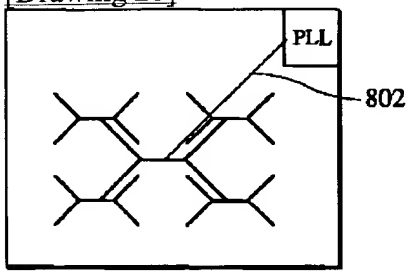
(b)



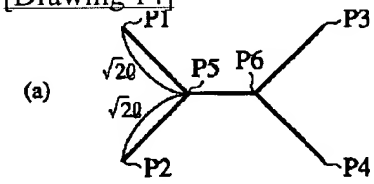
[Drawing 18]

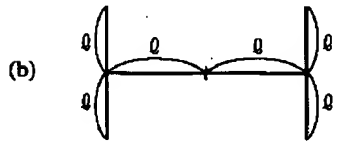


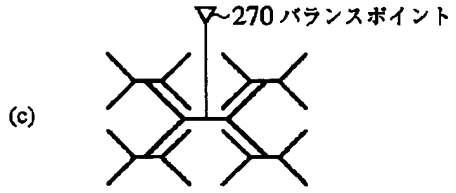
[Drawing 26]

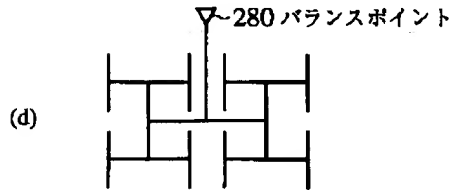


[Drawing 14]



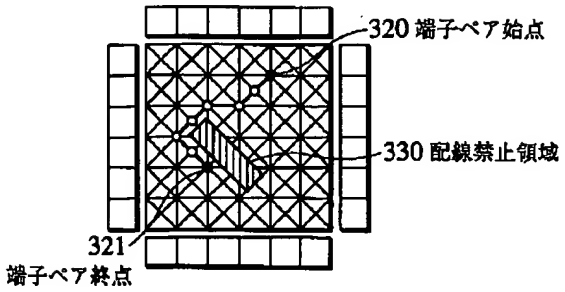




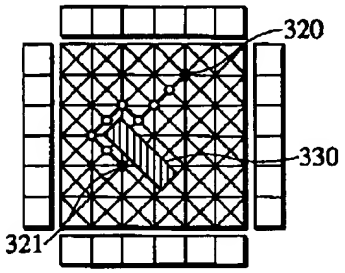


[Drawing 17]

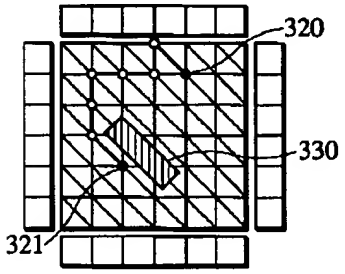
(a)



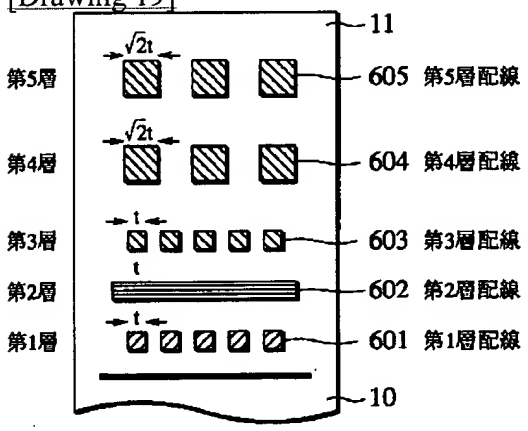
(b)



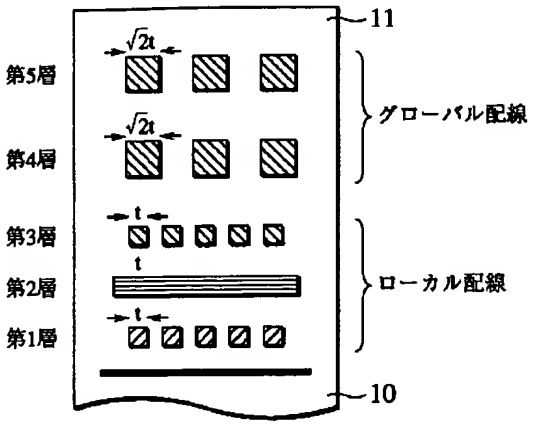
(c)



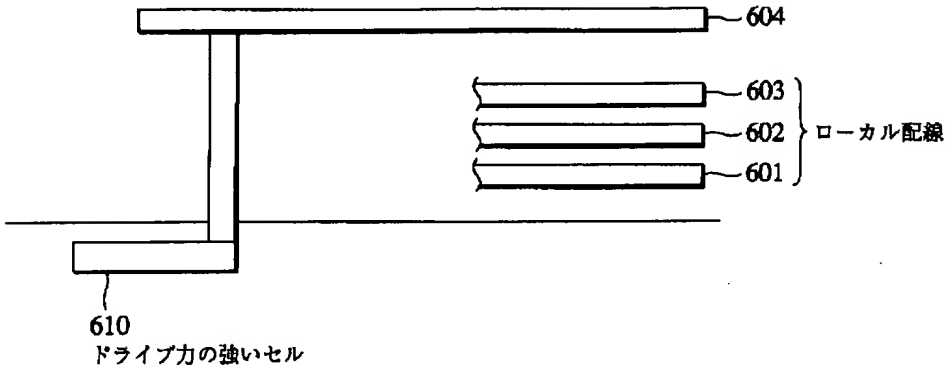
[Drawing 19]



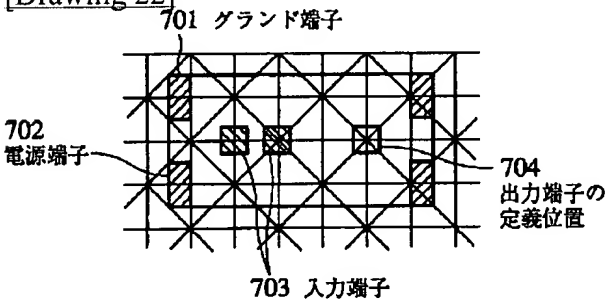
[Drawing 20]



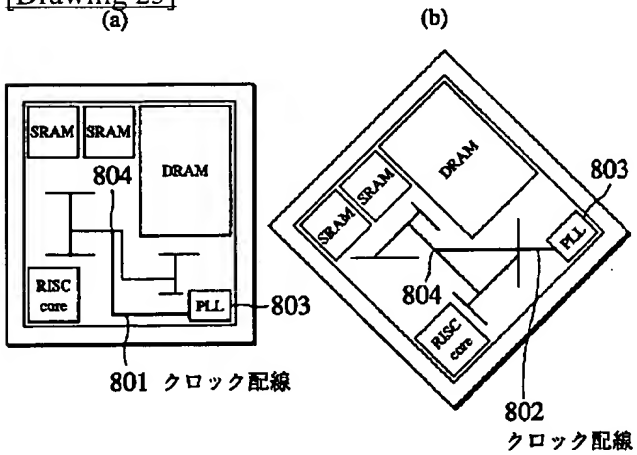
[Drawing 21]



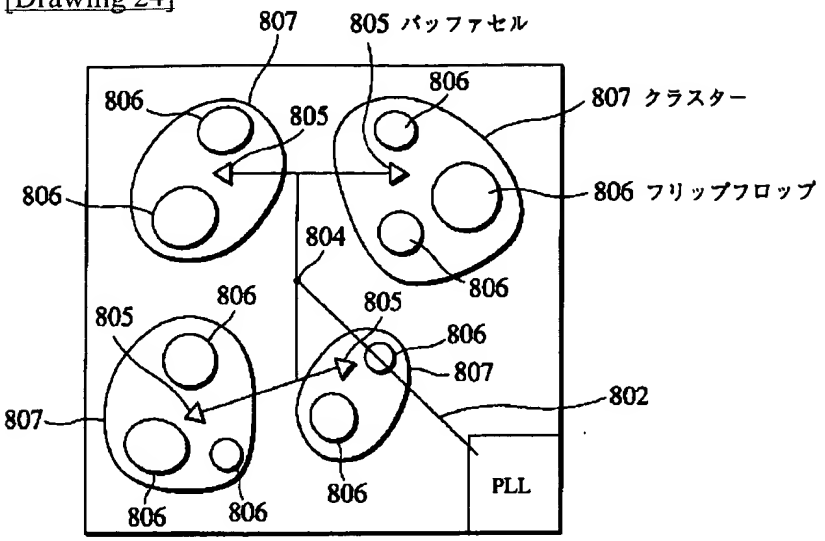
[Drawing 22]



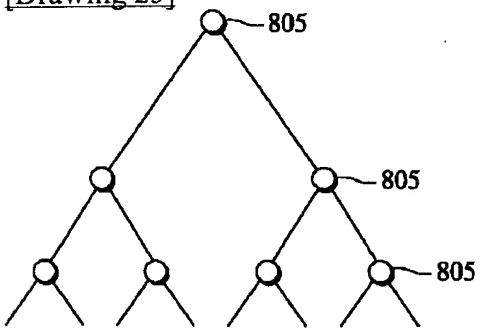
[Drawing 23]



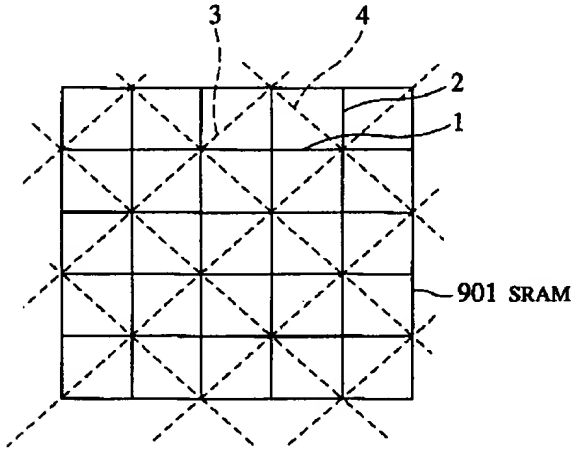
[Drawing 24]



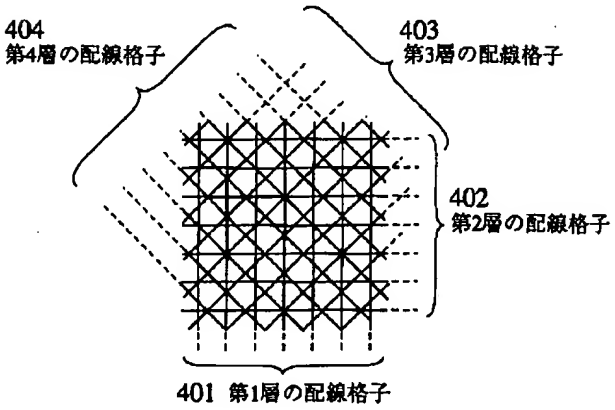
[Drawing 25]



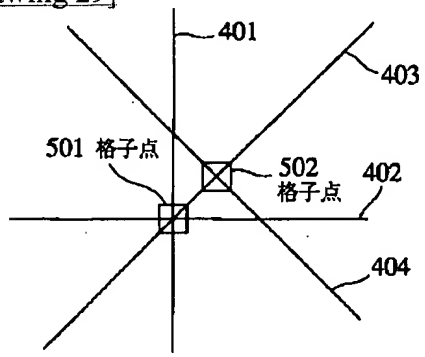
[Drawing 27]



[Drawing 28]



[Drawing 29]



[Translation done.]